DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program– M.Tech VLSI

(Applicable from the academic year 2025-2026)

Program: **M. Tech VLSI**

Regulation: R25

I Year I Semester-Course Structure

S.No	Category	Course Code	Course Title	L	T	P	Credits
1.	PC	R25D57101	**Professional Core - I** CMOS Digital IC Design	3	0	0	3
2.	PC	R25D57102	**Professional Core - II** CMOS Analog IC Design	3	0	0	3
3.	PE	R25D57103 R25D57104 R25D57105	**Professional Elective - I** 1. Device Modeling 2. Embedded Real Time Operating Systems 3. Nano materials and Nanotechnology	3	0	0	3
4.	PE	R25D57106 R25D57107 R25D57108	**Professional Elective - II** 1. Machine Learning and Deep Learning 2. VLSI Architectures for Digital Signal Processing 3. Scripting Languages for Design Automation	3	0	0	3
5.	PC	R25D57109	**Laboratory-I** CMOS Digital IC Design Laboratory	0	0	4	2
6.	PC	R25D57110	**Laboratory-II** CMOS Analog IC Design Laboratory	0	0	4	2
7.	CC	R25MBA101	**Compulsory Course** Research Methodology & IPR	2	0	0	2
8.	AC	R25BS101 R25BS102	**Audit Course – I** 1 English for Research Paper Writing 2 Disaster Management	2	0	0	0
			Total	**16**	**0**	8	**18**

Category	Courses	Credits
Professional Core Course	04	10
Professional Elective Course	02	06
Compulsory Course	01	02
Audit Course	01	0
Total	**08**	**18**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Program: M.Tech VLSI
Regulations- R25
I Year II Semester - Course Structure

S.No.	Category	Course Code	Course Title	L	T	P	Credits
1.	PC	R25D57201	**Professional Core - III** Mixed Signal IC Design	3	0	0	3
2.	PC	R25D57202	**Professional Core - IV** FPGA Based System Design	3	0	0	3
3.	PE	R25D57203 R25D57204 R25D57205	**Professional Elective - III** 1. VLSI Test and Testability 2. Physical Design Automation with AI 3. Functional Verification using System Verilog and UVM	3	0	0	3
4.	PE	R25D57206 R25D57207 R25D57208	**Professional Elective - IV** 1. Low Power VLSI Design 2. Microchip Fabrication Techniques 3. Power Management IC Design	3	0	0	3
5.	PC	R25D57209	**Laboratory-III** Mixed Signal IC Design Laboratory	0	0	4	2
6.	PC	R25D57210	**Laboratory-IV** FPGA Based System Design Laboratory	0	0	4	2
7.	PJ	R25D57211	Mini Project with Seminar	0	0	4	2
8.	AC	R25MBA201 R25MBA202	**Audit Course- II** 1 Constitution of India 2 Pedagogy Studies	2	0	0	0
			Total	**14**	**0**	**12**	**18**

Category	Courses	Credits
Professional Core	04	10
Professional Elective	02	06
Project	01	02
Audit Course	01	0
Total	**08**	**18**

Chairperson
Board of Studies (ECE)

R25D57101 **CMOS DIGITAL IC DESIGN** **3 0 0 3**

Course Objectives:

1.Understand CMOS Inverter Fundamentals
2. Explore Combinational Logic Design Styles
3. Develop Sequential Logic Circuit Knowledge
4. Examine Digital IC Implementation Strategies
5. Analyze Interconnect Effects in VLSI Systems

Course Code	Course Outcomes		Mapping with POs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Analyze static and dynamic behavior of CMOS inverters using key performance metrics.	3	2	2	1	1	1	-	L1,L2
C02	Design combinational logic circuits using static and dynamic CMOS styles.	3	3	1	2	1	-	-	L2,L4
C03	Implement various sequential logic elements and pipelining techniques.	3	2	2	2	1	-	1	L3,L4
C04	Apply custom and semi-custom design methodologies for digital ICs.	2	3	2	3	1	-	1	L2,L4,L5
C05	Evaluate interconnect effects and apply techniques to reduce parasitic impact.	3	1	2	2	1	2	-	L1,L5

Syllabus

Unit I:

The CMOS Inverter: Introduction, the static CMOS inverter, Evaluating the robustness of the CMOS inverter – static behavior, Performance of CMOS inverter – dynamic behavior, Power, energy and energy-delay, Technology scaling and its impact on the inverter metrics.

Unit II:

Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS design – complementary CMOS, ratioed logic, pass-transistor logic, Dynamic CMOS design – basic principles, speed and power dissipation of dynamic logic, Issues in dynamic design, cascading dynamic gates, Choosing a logic style, Designing logic for reduced supply voltage.

Unit III:

Designing Sequential Logic Circuits: Introduction – timing metrics for sequential circuits,Classification of memory elements, Static latches and registers – bistability principle, multiplexer-based latches, master-slave edge-triggered register, Low-voltage static latches, static SR flip-flops, Dynamic latches and registers – transmission gate edge-triggered registers, C2MOS, TSPCR, Pipelining – latch vs. register-based pipelines, NORA-CMOS

Unit IV:

Implementation Strategies for Digital ICs: Introduction, From custom to semi-custom and structured array design approaches, Custom circuit design, Cell-based design methodology, Array-based implementation approaches.

Unit V:

Coping with Interconnect: Introduction, Capacitive parasitics, Resistive parasitics, Inductive parasitics, Advanced interconnect techniques.

Self-Learning Topics:

1.High-speed logic design in FinFET and multi-threshold CMOS

2. Optical interconnects and 3D IC integration

Board of Studies: Electronics and Communication Engineering

Approved in BOS No: 01,08th September2025

Approved in ACM No: 01

TEXTBOOKS:

- Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed., Pearson Education, 2003.

REFERENCEBOOKS:

- Kang, Sung-Mo (Steve), and Yusuf Leblebici. CMOS Digital Integrated Circuits: Analysis and Design. 3rd ed., McGraw-Hill, 2003.
- 2. Uyemura, John P. Introduction to VLSI Circuits and Systems. Wiley, 2002.
- 3. Weste, Neil H.E., and David Harris. CMOS VLSI Design: A Circuits and Systems Perspective. 4th ed., Pearson Education, 2011.

Web References:

1. https://www.Analog CMOS circuits.com/
2. https://nptel.ac.in/courses/108/107/108105958/
3. https://electronics CMOS Circuit design & Layout.ws/
4. https://www.DIGITAL IC-notes.com/

E-Books:

1. CMOS VLSI Design: A Circuits and Systems Perspective
2. CMOS: Circuit Design, Layout, and Simulation (3rd / 4th Edition)
3. **"**Fundamentals of Modern VLSI Devices**"** by Yuan Taur
4. CMOS Analog IC Design: Fundamentals&Learning by Problem Solving
5. **"**Practice Problems for Hardware Engineers**"**

Internal Assessment Pattern

Cognitive Level	**Internal Assessment #1(%)**	**Internal Assessment #2(%)**
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

1. Define noise margins of a CMOS inverter.
2. List the metrics used to evaluate the robustness of CMOS inverters.
3. What is ratioed logic?
4. State the advantages of complementary CMOS logic.
5. List the different classifications of memory elements in sequential circuits.
6. Define bistability principle in latches.
7. What is C2MOS register?

L2 – Understand

1. Explain the static and dynamic behavior of a CMOS inverter.
2. Describe the impact of technology scaling on inverter delay and energy.
3. Explain the principle of pass-transistor logic with an example.
4. Compare static CMOS and dynamic CMOS design styles.
5. Explain the working of master–slave edge-triggered registers.

L3 – Apply

1. Calculate the noise margins of a CMOS inverter given device parameters.
2. Derive the delay expression of a CMOS inverter considering load capacitance.
3. Implement a full adder using complementary CMOS logic.
4. Show how cascading dynamic gates may lead to charge-sharing issues.
5. Design a multiplexer-based latch and explain its operation.

L4 – Analyze

1. Analyze the trade-off between static and dynamic power in CMOS inverters.
2. Compare complementary CMOS, ratioed logic, and pass-transistor logic in terms of area, delay, and power.
3. Differentiate between low-voltage static latches and conventional static latches.
4. Analyze the stability issues in dynamic latches and registers.
5. Compare pipeline performance in latch-based vs register-based designs.

L5 – Evaluate/Create

1. Justify why CMOS inverter is considered the fundamental building block in VLSI design.
2. Evaluate the robustness of pass-transistor logic compared to static CMOS logic.
3. Assess the speed and power trade-offs in dynamic CMOS design.
4. Judge the suitability of master-slave registers for low-power applications.
5. Evaluate the advantages and disadvantages of NORA-CMOS pipelining.

Chairperson

Board of Studies (ECE)

R25D57102 **CMOS ANALOG IC DESIGN 3 0 0 3**

Course Objectives:

1.Understand MOS Device Physics
2. Introduce Single-Stage Amplifiers
3. Develop Differential Amplifier Concepts
4. Explore Current Mirror Architectures
5. Design and Evaluate Operational Amplifiers

CourseCode	Course Outcomes		MappingwithPOs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Apply MOS device characteristics and second-order effects to analog circuit analysis	3	2	2	1	1	1	-	L1,L2
C02	Design single-stage MOS amplifier configurations for specific gain and impedance requirements	3	3	1	2	1	-	-	L2,L4
C03	Analyze the performance of differential amplifiers under common-mode and differential-mode operation.	3	2	2	2	1	-	1	L3,L4
C04	Apply current mirror topologies to design biasing circuits in CMOS analog design	2	3	2	3	1	-	1	L2,L4,L5
C05	Compare operational amplifier topologies considering gain, bandwidth, and power trade-offs.	3	1	2	2	1	2	-	L1,L5

Syllabus:

Unit I:

MOS Device Physics and Models:Introduction to analog design, MOS device physics – General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Unit II:

Single Stage Amplifiers: Basic Concepts, Common-Source Stage with resistive-load and diode connected load, Source Follower, Common-Gate Stage.

Unit III:

Differential Amplifiers: Single-Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Mode with MOS Loads, Gilbert Cell.

Unit-IV

Passive and Active Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors

Unit-V:

Operational Amplifiers: General Considerations, One-Stage Op Amps, Two-Stage Op Amps, Gain Boosting, Comparison.

Self-Learning Topics:

1.Advanced Device Modeling & Short-Channel Effects

2. CMOS Op-Amp Architectures

Board of Studies: Electronics and Communication Engineering

Approved in BOS No: 01,08th September2025

Approved in ACM No: 01

TEXTBOOKS:

- Razavi, Behzad. Design of Analog CMOS Integrated Circuits. McGraw-Hill Education, 2001.

REFERENCEBOOKS:

- Allen, Philip E., and Douglas R. Holberg. CMOS Analog Circuit Design. 3rd ed., Oxford University Press, 2011.
- 2. Johns, David A., and Ken Martin. Analog Integrated Circuit Design. Wiley India, 2015.
- 3. Sansen, Willy M.C. Analog Design Essentials. Springer, 2006.

Web References:

1. https://www.Analog CMOS Integrated circuits.com/
2. https://nptel.ac.in/courses/108/107/108105958/
3. https://electronics CMOS Circuit design & Layout.ws/
4. https://www.Arm microcontroller-notes.com/

E-Books:

1. Design of Analog CMOS Integrated Circuits
2. CMOS: Circuit Design, Layout, and Simulation (3rd / 4th Edition)
3. CMOS Analog Circuit Design (2nd / 3rd Edition)
4. CMOS Analog IC Design: Fundamentals&Learning by Problem Solving
5. Analog Integrated Circuit Design

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

1. Define threshold voltage of a MOS transistor.
2. List the second-order effects in MOSFETs.
3. List the types of single-stage amplifiers using MOS.
4. Define transconductance (gm) and output resistance (ro).
5. Define differential mode gain.
6. What is common-mode rejection ratio (CMRR)?
7. Define current mirror.

L2 – Understand

1. Explain the I–V characteristics of a MOSFET in different regions of operation.
2. Discuss the importance of MOS device modeling in analog design.
3. Explain the operation of a source follower.
4. Describe the small-signal model of a common-source stage.
5. Explain the working principle of a MOS differential pair.
6. Describe the concept of single-ended vs differential outputs.

L3 – Apply

1. Illustrate how channel-length modulation affects MOS transistor current.
2. Calculate the drain current for a given MOS transistor using square-law equation.
3. Apply small-signal analysis to derive the gain of a common-gate stage.
4. Show how diode-connected load improves amplifier linearity.
5. Calculate the CMRR of a given differential amplifier circuit.

L4 – Analyze

1. Compare long-channel and short-channel MOSFET models.
2. Analyse the impact of body effect on MOS threshold voltage.
3. Differentiate between resistive load and diode-connected load in CS amplifier.
4. Analyse the input and output impedance of a source follower.
5. Analyse the common-mode response of a MOS differential amplifier.

L5 – Evaluate/Create

1. Justify why short-channel effects degrade analog circuit performance.
2. Evaluate the suitability of MOSFETs over BJTs in modern analog design.
3. Evaluate the performance of CS, CG, and CD stages in terms of gain, input, and output impedance.
4. Evaluate the significance of the Gilbert Cell in RF applications.
5. Judge the trade-off between gain and linearity in a differential amplifier.

Chairperson

Board of Studies (ECE)

R25D57103 DEVICE MODELLING (PE - I) 3 0 0 3

Course Objectives:

1. To obtain the functional relationship among the terminal electrical variables of the device that is to be modeled
2. To know the physical properties of materials and devices
3. To know the MOS transistor low frequency model
4. To Study the operation and characteristics of key devices like diodes, transistors, and MOSFETs.
5. To Understand the impact of scaling and short-channel effects in modern devices.

Course Code	Course Outcomes	Mapping with POs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Explain the physical structure and electrical behaviour of MOSFET devices.	3	3	2	2	1	1	-	L1,L2
C02	Analyse and model MOS capacitors and threshold voltage characteristics.	3	3	2	2	1	-	-	L2,L3
C03	Develop current-voltage and capacitance models for MOSFETs.	3	3	3	2	1	-	-	L2,L3
C04	Evaluate device reliability issues and implement SPICE-based models.	3	3	3	2	1	-	-	L2,L3
C05	Apply parameter extraction techniques and statistical modeling in circuit simulation	3	3	3	3	2	-	-	L3,L4

Syllabus:

UNIT-I

Fundamentals of MOSFET Structure and Device Physics: Review of semiconductor physics and p–n junction, MOS transistor structure and operation, Scaling effects and parasitics, Modern VLSI device structures.

UNIT- II

MOS Capacitor and Threshold Voltage Modeling: MOS capacitor - physics and C–V characteristics, Threshold voltage modeling: uniform and nonuniform doping, Short-channeleffects: DIBL, narrow-width effect, Temperature dependence of threshold voltage

UNIT- III

DC and Dynamic Modeling of MOSFETs: Charge-sheet and Pao–Sah current models, Subthreshold conduction and mobility degradation, Temperature effects on current characteristics,Capacitance models: Meyer model, charge-based model, Small-signal modeling

UNIT-IV

Reliability Modeling and SPICE Device Models: Hot-carrier degradation and reliability concerns, Gate and substrate currents, SPICE MOSFET models: LEVEL 1, 2, 3, Parameter definitions and usage in simulation

UNIT-V

Parameter Extraction and Statistical Modeling: Measurement techniques: C–V, threshold voltage, mobility, Parameter extraction using optimization techniques, Statistical modeling for process variation, Worst-case modeling in VLSI design**.**

Self-Learning Topics: Parameter extraction using optimization techniques
Board of Studies: Electronics and Communication Engineering
Approved in BOS No:01,08th September2025
Approved in ACM No: 01

TEXTBOOKS:

1. Arora, Narain. MOSFET Modeling for VLSI Simulation: Theory and Practice. Springer Science& Business Media, 2007.

REFERENCE BOOKS

1. Tsividis, Yannis, and Colin McAndrew. Operation and Modeling of the MOS Transistor. 3rd ed., Oxford University Press, 2011.
2. Sze, S. M., and Kwok K. Ng. Physics of Semiconductor Devices. 3rd ed., Wiley, 2006.
3. Trivedi, Subarna S., and Saurabh Kumar Gupta. Semiconductor Device Modeling andTechnology. PHI Learning, 2012.
4. Muller, Richard S., and Theodore I. Kamins. Device Electronics for Integrated Circuits. 3rded., Wiley, 2002.

Web References:

1. **https://www.worldscientific.com/**
2. **https://onlinecourses.nptel.ac.in/noc23_ee35/preview**
3. **https://www.scribd.com/document/522085652/Robert-E-Miles-Auth-Christopher-M-Snowden**
4. **https://link.springer.com/chapter/10.1007/978-1-4615-2297-3_3**

eBooks:

1. Fundamentals of Modern VLSI Devices": Look for the 3rd edition published in 2022.
2. S. M. Sze, Physics of Semiconductor Devices, John Wiley & Sons.
3. Operation and Modeling of the MOS Transistor – Yannis P. Tsividis

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define device modelling.
- State Poisson's equation used in semiconductor device modelling.
- List two common MOSFET models used in VLSI design.
- Write the expression for drain current in the saturation region of a MOSFET.
- List advanced devices that require new modelling approaches.

L2 – Understand

- Explain the need for device modelling in VLSI circuit design.
- Differentiate between physical models and compact models.
- Describe the limitations of long-channel MOSFET models when applied to short-channel devices.
- Explain why FinFETs require different modelling compared to planar MOSFETs.
- Why is parameter extraction crucial in compact modelling?

L3 – Apply

- Apply the **drift-diffusion model** to calculate the current density in a semiconductor device given carrier concentration and mobility.
- For a given **BJT structure**, apply the Ebers-Moll model to calculate the collector current at a specific base-emitter voltage.
- Apply the **small-signal model of MOSFET** to determine transconductance (gmg_mgm) and output resistance (ror_oro) for given biasing conditions.
- Using **channel length modulation concept**, compute the drain current of a MOSFET operating in the saturation region.
- For a specified **semiconductor doping profile**, apply modeling techniques to extract depletion width and junction capacitance.

L4 – Analyze

- Analyze the impact of **channel length modulation** on the output characteristics of a MOSFET and explain how it deviates from the ideal saturation model.
- Compare and analyze the **I-V characteristics** of a Schottky diode and a PN junction diode under forward and reverse bias conditions.
- Given a **high-frequency BJT model**, analyze the role of parasitic capacitances in limiting the cut-off frequency (fTf_TfT) and maximum oscillation frequency (fmaxf_{max}fmax).
- Break down the **drift and diffusion current components** in a PN junction diode under forward bias and analyze which dominates at different injection levels.
- For a given MOSFET, analyze how **oxide thickness scaling** influences threshold voltage, subthreshold leakage, and gate capacitance.

L5 – Evaluate/Create

- Evaluate the **limitations of the Shockley ideal diode equation** when applied to real diodes at high injection levels.
- Compare and evaluate the **Ebers–Moll model vs. Gummel–Poon model** for BJT device modelling in terms of accuracy and complexity.
- Develop a **modified diode model** that accounts for recombination–generation current in the depletion region.
- Create a **simulation workflow** to extract threshold voltage and mobility parameters from experimental MOSFET I–V characteristics.

Chairperson
Board of Studies (ECE)

R25D57104 EMBEDDEDREALTIMEOPERATINGSYSTEMS (PE - I) 3 0 0 3

Course Objectives:

1. ToprovidebroadunderstandingoftherequirementsofRealTimeOperatingSystems.
2. TomakethestudentunderstandapplicationsoftheseRealTimefeaturesusingcasestudies.
3. Develop the ability to design, implement, and analyze embedded systems using real-time operating systems.
4. Expose students to industry-standard RTOS (e.g., FreeRTOS, VxWorks, RTLinux, or similar) for practical embedded applications.
5. Enable students to evaluate performance, reliability, and real-time constraints in embedded application

Course Code	Course Outcomes	MappingwithPOs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Analyse key concepts and roles of real-time operating systems in embedded system design.	3	2	1	2	1	1	-	L1,L2
C02	Evaluate task scheduling and synchronization methods in real-time systems.	3	3	3	2	2	1	-	L2,L3
C03	Design interrupt and timer handling mechanisms for embedded real-time environments	2	3	3	3	2	-	-	L2,L3
C04	Apply real-time memory management techniques in embedded applications.	2	3	3	3	3	2	3	L1,L4
C05	Create modular real-time applications to resolve deadlocks and priority inversion	3	3	1	2	3	-	-	L4,L5

Syllabus:

UNIT-I

Introduction to RTOS: Real life examples of embedded systems, real-time embedded systems, the future of embedded systems, a brief history of operating systems, defining an RTOS, the scheduler, objects, services, key characteristics of an RTOS.

UNIT- II

Tasks: Introduction, defining a task, task states and scheduling, typical task operations, typical task structure, synchronization, communication, and concurrency.

Semaphores: Introduction, defining semaphores, typical semaphore operations, typical semaphoreuse.

Message Queues: Introduction, defining message queues, message queue states, message queuecontent, message queue storage, typical message queue operations, and typical message queue use**.**

UNIT- III

Exceptions and Interrupts: Introduction, what are exceptions and interrupts, a closer look at exceptions and interrupts, processing general exceptions, the nature of spurious interrupts.

Timer and Timer Services: Introduction, real-time clocks and system clocks, programmable interval timers, timer interrupt service routines, a model for implementing the soft-timer handling facility, timing wheels, soft timers and timer related operations.

UNIT-IV

Memory Management: Introduction, dynamic memory allocation in embedded systems, fixed-size memory management in embedded systems, blocking vs. non-blocking memory functions, hardware memory management units.

UNIT-V

Modularizing Applications: Introduction, an outside-in approach to decomposing applications, guidelines and recommendations for identifying concurrency, schedulability analysis – rate monotonic analysis.

Common Design Problems: Introduction, resource classification, deadlocks, priority inversion.

Self-Learning Topics: Resource sharing and priority inheritance protocols

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01,08th September2025

Approved in ACM No: 01

TEXTBOOK:

1. Qing Li, and Caroline Yao. Real-Time Concepts for Embedded Systems. CMP Books, 2003.

REFERENCEBOOKS:

1. Prasad, K. V. K. K. Embedded Real-Time Systems: Concepts, Design & Programming. DreamTech Press, 2005.
2. Simon, David E. An Embedded Software Primer. 1st ed., 5th impression, Addison-WesleyProfessional, 2007.
3. Singh, Rajib Mall. Real-Time Systems: Theory and Practice. Pearson Education India, 2006.

Web References:

1. https://www.Real time embedded systems.com/
2. https://nptel.ac.in/courses/108/105/108105158/
3. https://electronics-tutorials.ws/
4. https://www Moschip RTOS-notes.com/
5. https://www.UCSD processors.com/

E-Books:

1. A Practical Introduction to Real-Time Operating Systems Douglas Wilhelm Harder, Jeff Zarnett, VajihMontaghami, et al.
2. Hands-On RTOS with Microcontrollers Brian Amos
3. Real-Time Operating System in Embedded Systems

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define a Real-Time Operating System (RTOS).
- List different types of tasks in an RTOS (periodic, aperiodic, sporadic).
- Recall the difference between hard and soft real-time systems.
- State the purpose of semaphores and mutexes.
- Name popular RTOS used in embedded systems.

L2 – Understand

- Explain the difference between general-purpose OS and RTOS.
- Describe how context switching works in an RTOS.
- Interpret the importance of task priorities in scheduling.
- Explain why priority inversion occurs and how it can be mitigated.
- Summarize the functions of message queues and event flags.

L3 – Apply

- Apply fixed-priority scheduling to a set of tasks and determine the execution order.
- Implement a producer-consumer problem using semaphores in FreeRTOS.
- Calculate CPU utilization for a given set of periodic tasks.
- Apply inter-task communication mechanisms for a sensor-data collection system..

L4 – Analyze

- Analyze the effect of task blocking on real-time performance.
- Examine the trade-offs between static and dynamic memory allocation in RTOS.
- Analyze how jitter affects the performance of periodic tasks.
- Examine task synchronization issues in multi-core RTOS systems.

L5 – Evaluate/Create

- Evaluate the suitability of FreeRTOS vs VxWorks for an automotive control system.
- Critically assess the impact of priority inheritance protocols on system performance.
- Judge the effectiveness of different inter-task communication mechanisms for a given application.
- Evaluate design trade-offs for memory usage vs task responsiveness in an RTOS.
- Recommend an RTOS design strategy for low-power IoT devices and justify your choice.

Chairperson
Board of Studies (ECE)

R25D57105 NANOMATERIALS AND NANOTECHNOLOGY(PE - I) 3 0 0 3

Course Objectives:

1. **To Introduce the fundamentals** of nanoscience and nanotechnology, including concepts of size, dimensionality, and unique properties of nanomaterials.
2. **To Understand synthesis methods** of nanomaterials (top-down and bottom-up approaches, physical, chemical, and biological techniques).
3. **Explain the structural, optical, electrical, and mechanical properties** of nanomaterials and how they differ from bulk materials.
4. **Familiarize students with characterization techniques** (SEM, TEM, AFM, XRD, Raman spectroscopy, etc.) used to study nanostructures.
5. **Explore various types of nanomaterials** (carbon nanotubes, nanowires, quantum dots, graphene, nanoparticles, etc.) and their applications.

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Analyse key concepts and roles of real-time operating systems in embedded system design.	3	2	1	2	1	1	-	L1,L2
C02	Explain the various synthesis methods for nanostructures and their suitability for scaling applications.	3	3	3	2	2	1	-	L2,L3
C03	Illustrate the working principles and fabrication processes of MEMS and nanolithography techniques.	2	3	3	3	2	-	-	L2,L3
C04	Analyse the growth mechanisms, properties, and applications of carbon nanotubes (CNTs).	2	3	3	3	3	2	3	L1,L4
C05	Evaluate the emerging applications of advanced nanomaterials in electronics, biology, andenvironmental fields.	3	3	1	2	3	-	-	L4,L5

Syllabus:

UNIT-I

Introduction to Nanomaterials and Nanotechnologies: Features of nanostructures, Applicationsof nanomaterials and technologies, Nano-dimensional materials 0D, 1D, 2D structures, Size effects, Fraction of surface atoms, Specific surface energy, Surface stress, Effect on the lattice parameter, Phonon density of states, General methods for synthesis of nanostructures, Precipitative methods, Reactive methods, Hydrothermal/solvothermal methods, Suitability of synthesis methods forscaling, Potential uses.

UNIT- II

Fundamentals and Classification of Nanomaterials: Classification of nanomaterials, Zero dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three-dimensional nanomaterials, Low-dimensional nanomaterials and applications, Synthesis, properties and applications of low-dimensional carbon-related nanomaterials.

UNIT- III

Micro- and Nanolithography Techniques and MEMS: Micro- and nanolithography techniques, Emerging applications, Introduction to MEMS, Advantages and challenges of MEMS, Fabrication technologies, Surface micromachining, Bulk micromachining, Molding, Introduction to nanophotonic.

UNIT-IV

Carbon Nanotubes (CNTs): Introduction to CNTs, Synthesis of CNTs (arc-discharge, laser ablation,catalytic growth), Growth mechanisms of CNTs, multi-walled nanotubes, Single-walllednanotubes, Optical properties of CNTs, Electrical transport in perfect nanotubes, Applications of CNTs.

UNIT-V

Advanced Nanomaterials and Applications: Ferroelectric materials, Coating, Molecular electronics, Nanoelectronics, Biological and environmental applications, Membrane-based applications, Polymer-based applications.

Self-Learning Topics: Resource sharing and priority inheritance protocols

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01,08th September2025

Approved in ACM No: 01

TEXTBOOK:

1. Gusev and A. A. Rempel. Nanocrystalline Materials. Cambridge International SciencePublishing; 1st Indian edition, Viva Books Pvt. Ltd., 2008.
2. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, and James Murday. Nanoscience and Nanotechnology. Tata McGraw-Hill Education, 2012.

REFERENCEBOOKS:

1. Kenneth J. Klabunde and Ryan M. Richards, editors. Nanoscale Materials in Chemistry. 2nded., John Wiley & Sons, 2009.
2. Bharat Bhushan. Springer Handbook of Nanotechnology. 3rd ed., Springer, 2010.
3. Kamal K. Kar. Carbon Nanotubes: Synthesis, Characterization and Applications. 1st ed., Research Publishing Services, 2011.

WEB REFERENCES:

1. https://mrforum.com/product/applications-of-emerging-nanomaterials-and nanotechnology

2. https://onlinelibrary.wiley.com/journal/nax
3. https://www.eolss.net/ebooklib/bookinfo/nanoscience-nanotechnologies.aspx
4. https://www.intechopen.com/series/26

E-Books:

1. Nano: The Essentials – Understanding Nanoscience and Nanotechnology by T. Pradeep (IIT-Madras).
2. Nanomaterials and Nanotechnology (Peng & Li)
3. Nanomaterials: Introduction and Applications.

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define **carbon nanotubes (CNTs)**.
- What is meant by **surface-to-volume ratio** in nanomaterials?
- Name two **applications of nanotechnology in medicine**.
- What is meant by **nanocomposite**?
- Write the principle of **X-ray Diffraction (XRD)** used in nanomaterial characterization.

L2 – Understand

- Explain the importance of surface-to-volume ratio in nanostructures.
- Why does quantum confinement lead to changes in the band gap of nanoparticles?
- Compare physical, chemical, and biological methods of nanoparticle synthesis.
- Explain the difference between scanning electron microscopy (SEM) and transmission electron microscopy (TEM).
- Discuss why carbon nanotubes are considered potential candidates for nanoelectronics.

L3 – Apply

- Design an experiment to synthesize silver nanoparticles using a green synthesis method and explain how you would confirm their formation.
- Given the bandgap shift in quantum dots, explain how you would tune the emission color for a display application.
- A biomedical company wants to use gold nanoparticles for targeted cancer therapy. Suggest how nanomaterials can be used for drug delivery.
- You are asked to improve the strength-to-weight ratio of an aircraft wing. Which type of nanocomposite would you choose, and why?
- Apply the concept of nanostructured catalysts to improve the efficiency of a chemical reaction in the petroleum industry.

L4 – Analyze

- Compare and contrast top-down and bottom-up methods of nanoparticle synthesis in terms of cost, scalability, and quality control.
- Examine how the quantum confinement effect influences the optical properties of nanoparticles.
- Analyze the role of surface functionalization in improving the stability of nanomaterials in biological applications.
- Differentiate between scanning electron microscopy (SEM) and atomic force microscopy (AFM) in terms of resolution, sample preparation, and applications.
- A company wants to choose between metal-oxide nanoparticles and carbon-based nanomaterials for gas sensing. Analyze the advantages and limitations of each.

L5 – Evaluate/Create

- Evaluate the effectiveness of **carbon nanotubes vs. silicon nanowires** for use in future nanoelectronics.
- Critically assess the **advantages and risks** of using **nanoparticles in food and cosmetics**.
- Justify the selection of **graphene-based electrodes** over conventional electrodes in supercapacitors.
- Design a **nano-enabled drug delivery system** to target only cancer cells without affecting healthy tissue.
- Propose a **nanomaterial-based water filtration system** for rural areas with limited resources.

Chairperson

Board of Studies (ECE)

R25D57106 **MACHINE LEARNING AND DEEP LEARNING 3 0 0 3**

Course Objectives:

1. Foundations of Machine Learning
2. Deep Neural Network Fundamentals
3. Regularization and Optimization
4. Advanced Architectures
5. Practical Applications of Deep Learning

Course Code	Course Outcomes		Mapping with POs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Analyze machine learning algorithms and evaluate model performance using concepts like overfitting, bias-variance, and likelihood-based estimation.	3	2	2	1	1	1	-	L1,L2
C02	Designdeep feedforward neural networks using appropriate architectures, activation functions, and backpropagation techniques.	3	3	1	2	1	-	-	L2,L4
C03	Apply regularization and optimization techniques to improve generalization and training efficiency of deep neural networks.	3	2	2	2	1	-	1	L3,L4
C04	Implement convolutional and recurrent neural network models for processing spatial and sequential data.	2	3	2	3	1	-	1	L2,L4,L5
C05	Evaluatemodel performance and deployment strategies in real-world applications such as computer vision, NLP, and speech recognition.	3	1	2	2	1	2	-	L1,L5

Syllabus:

Unit-I:

Machine Learning Basics:Learning algorithms, Capacity, overfitting and underfitting, estimators, bias and variance, maximum likelihood estimation, Bayesian statistics, Supervised and unsupervised learning algorithms, building a machine learning algorithm, challenges motivating deep learning.

Unit-II:

Deep Feedforward Networks: Gradient-based learning, hidden units, architecture design, back propagation and other differentiation algorithms.

Unit-III:

Regularization for Deep Learning:Norm penalties, Dataset augmentation, multi-task learning, early stopping, sparse representations, ensemble methods, dropout.**Optimization**: Optimization for Training Deep Models, challenges in neural network optimization, basic algorithms, parameter initialization strategies, algorithms with adaptive learning rates.

Unit-IV:

Convolutional Neural Networks:The convolution operation, motivation, pooling, convolution and pooling as an infinitely strong prior, variants of the basic convolution function, structures outputs, data types, efficient convolution algorithms, random or unsupervised features.

Sequence Modeling: Recurrent and Recursive Nets, Recurrent Neural Networks, Recursive Neural Networks, Long Short-Term Memory, optimization for long-term dependencies.

Unit-V:

Practical Methodology: Performance metrics, selecting hyperparameters, debugging strategies. Applications: Large-scale deep learning, computer vision, speech recognition, natural language processing, other applications.

Self-Learning Topics:

1.AutoML (Automated Machine Learning) and its applications

2. Batch Normalization and Layer Normalization

Board of Studies: Electronics and Communication Engineering

Approved in BOS No: 01,08th September2025

Approved in ACM No: 01

TEXTBOOKS:

- Goodfellow, Ian, Yoshua Bengio, and Aaron Courville. Deep Learning. MIT Press, 2016.

REFERENCEBOOKS:

- Géron, Aurélien. Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow. 2nd ed., O'Reilly Media, 2019.
- Bishop, Christopher M. Pattern Recognition and Machine Learning. Springer, 2006.
- Chollet, François. Deep Learning with Python. 2nd ed., Manning Publications, 2021.

Web References:

1. https://towardsdatascience.com/optimizers-for-training-neural-network-59450d71caf6
2. https://towardsdatascience.com/understanding-the-bias-variance-tradeoff-165e6942b229
3. http://neuralnetworksanddeeplearning.com
4. http://introtodeeplearning.com/

E-Books:

1. Deep Learning by Ian Goodfellow, Yoshua Bengio & Aaron Courville
2. Dive into Deep Learning by Aston Zhang, Zachary C. Lipton, Mu Li & Alexander J. Smola
3. The Little Book of Deep Learning by Florent Fleuret
4. Mathematical Introduction to Deep Learning by Jentzen, Kuckuck & von Wurstem berger

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

1. Define overfitting and underfitting in machine learning.
2. List the differences between supervised and unsupervised learning.
3. Define backpropagation.
4. State different types of activation functions used in deep networks.
5. List different regularization techniques in deep learning.

L2 – Understand

1. Explain the concept of bias-variance tradeoff with examples.
2. Illustrate how maximum likelihood estimation is used in ML.
3. Explain gradient-based learning with an example.
4. Interpret the role of hidden units in feedforward networks.
5. Explain how dropout prevents overfitting.

L3 – Apply

1. Apply Bayesian statistics to classify data into two classes with a simple example.
2. Demonstrate how to build a simple learning algorithm using scikit-learn.
3. Implement a 3-layer feedforward network for MNIST classification.
4. Apply ReLU activation to improve convergence in training.
5. Apply data augmentation to improve performance of an image classifier.

L4 – Analyze

1. Compare supervised, unsupervised, and reinforcement learning with case studies.
2. Analyze the challenges that motivated the development of deep learning.
3. Differentiate between sigmoid and ReLU activations in terms of performance.
4. Analyze the vanishing gradient problem in deep networks.
5. Compare Adam, SGD, and RMSProp optimizers.

L5 – Evaluate/Create

1. Evaluate the performance of an ML algorithm when training and testing accuracies differ.
2. Justify the use of maximum likelihood over Bayesian estimation in certain applications.
3. Assess the effectiveness of architecture depth on model accuracy.
4. Critically evaluate the limitations of back propagation.
5. Evaluate the tradeoff between model complexity and generalization error.

Chairperson
Board of Studies (ECE)

R25D57107**VLSI ARCHITECTURES FOR DIGITAL SIGNAL PROCESSING3 0 0 3**

Course Objectives:

1. Fundamentals of Digital Signal Processing (DSP) systems, algorithms, and application demands.
2. Teach unfolding and folding transformations and their applications in multirate DSP systems.
3. UnderstandPresent fast convolution algorithms (Cook-Toom, Winograd, cyclic and iterated convolution) for computational efficiency.
4. Knowbit-level arithmetic architectures including serial/parallel multipliers, bit-serial filters, and redundant arithmetic.
5. Provide knowledge on data format conversion and redundancy handling in arithmetic architectures.

Course Code	Course Outcomes		MappingwithPOs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Identify typical DSP algorithms and analyze their computational requirements for efficient VLSI implementation.	3	2	2	2	1	1	-	L1,L2
C02	Compute iteration bounds and apply retiming techniques to optimize DSP data flow graphs for performance.	3	3	2	2	1	-	-	L2,L4
C03	Design pipelined and parallel FIR filters and utilize unfolding and folding methods for architectural transformations.	3	2	2	2	1	-	-	L3,L4
C04	Implement fast convolution methods and develop efficient bit-level and redundant arithmetic units for DSP systems.	2	3	3	2	2	-	1	L4,L5
C05	Evaluate and compare programmable DSP processor architectures for various application domains such as mobile and multimedia systems	1	2	3	1	1	-	1	L1,L6

Syllabus:

Unit I:

Introduction to Digital Signal Processing Systems: Introduction, typical DSP algorithms, DSP application demands and scaled CMOS technologies.

Iteration Bound:data-flow graph representations, loop bound, and iteration bound, algorithms for computing iteration bound.

Pipelining and Parallel Processing: Introduction, pipelining of FIR digital filters, parallel processing.
Retiming: Definitions and properties, solving systems of inequalities, retiming techniques.

Unit II:
Unfolding: An algorithm for unfolding, properties and applications of unfolding.
Folding: Folding transformation, register minimization techniques, folding of multi ratesystems
Unit III:
Fast Convolution: Introduction, Cook-Toom algorithm, Winograd algorithm, iterated convolution, cyclic convolution, design of fast convolution algorithm by inspection.

Unit IV:
Bit-Level Arithmetic Architectures: Introduction, parallel multipliers, bit-serial multipliers, bit serial filter design and implementation.
Redundant Arithmetic: Introduction, redundant number representations, carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures, data format conversion, redundance to nonredundant converter.

Unit V:
Programmable Digital Signal Processors: Introduction, evolution of programmable digital signal processors, important features of DSP processors, DSP processors for mobile and wireless communications, processors for multimedia signal processing.

Self-Learning Topics:

1.VLSI implementation challenges in high-speed DSP systems

2. Approximate computing techniques in DSP arithmetic.

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TEXTBOOKS

1. Parhi, Keshab K. VLSI Digital Signal Processing Systems: Design and Implementation. Wiley, 1999.

REFERENCEBOOKS:

1. V. K. Madisetti, VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis, IEEE Press, New York.
2. 2. Meyer-Baese, Uwe. Digital Signal Processing with Field Programmable Gate Arrays. 4th ed., Springer, 2014.
3. 3. S. Y. Kung, H. J. Whitehouse, VLSI and Modern Signal Processing, PrenticeHall.

Web References:

1. https://www.tutorialspoint.com/digital_signal_processing
2. https://nptel.ac.in/courses/117105135
3. https://dsp.stackexchange.com/
4. https://users.ece.gatech.edu/~bonnie/book/Tutorials
5. https://ece.iisc.ac.in/

E-Books:

1."The Scientist and Engineer's Guide to Digital Signal Processing" – Steven W. Smith
2."Digital Signal Processing: Principles, Algorithms, and Applications" – Proakis & Manolakis (4th Ed.)
3. "Digital Signal Processing" by Li Tan
4. "Signal Processing and Linear Systems" – B. P. Lathi

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

1. Define iteration bound in DSP systems.
2. List applications of pipelining in FIR filters.
3. Define unfolding and its applications.
4. List fast convolution algorithms.
5. Define cyclic convolution.

L2 – Understand

1. Explain the concept of retiming with an example.
2. Summarize how parallel processing improves DSP performance.
3. Explain register minimization in folded architectures.
4. Describe properties of unfolding.
5. Explain the Cook-Toom algorithm with example.

L3 – Apply

1. Compute the loop bound for a given DSP data-flow graph.
2. Apply pipelining to reduce the critical path of a FIR filter.
3. Apply unfolding to double the throughput of a FIR filter.
4. Use folding to implement a 4-tap filter with minimum registers.
5. Implement a 4-point cyclic convolution using DFT.

L4 – Analyze

1. Differentiate between iteration bound and loop bound.
2. Analyze the impact of technology scaling on DSP algorithms.
3. Compare folding and unfolding techniques in multirate DSP.
4. Analyze register minimization techniques in folded systems.
5. Differentiate between linear and cyclic convolution.

L5 – Evaluate/Create

1. Justify the need for retiming in DSP systems for low-power design.
2. Assess the trade-offs between pipelining and parallel processing.
3. Evaluate the performance improvements using unfolding.
4. Judge whether folding is suitable for high-speed DSP processors.
5. Evaluate the efficiency of Cook-Toom algorithm over direct convolution.

Chairperson

Board of Studies (ECE)

R25D57108 SCRIPTING LANGUAGES FOR DESIGN AUTOMATION 3 0 0 3

Course Objectives:

1. To **Linux Fundamentals**: Covers basic commands, file systems, and shell scripting, which is the foundational environment for most EDA tools.
2. To**Perl Scripting**: Focuses on file handling, regular expressions for pattern matching in reports, and building reusable modules.
3. **Tcl Scripting**: Explores Tcl language basics, controlling EDA tools via command interfaces, and automation tasks like simulation control and report generation.
4. **Python Scripting**: Introduces Python fundamentals, object-oriented concepts, and advanced applications for data analysis and complex automation.
5. **Practical Applications in VLSI**: Hands-on projects combining the learned scripting languages to automate real-world front-end and back-end VLSI design flows.

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Describe the role of scripting languages in EDA workflows and differentiate between scriptingand compiled languages.	3	2	1	1	2	1	-	L1,L2
C02	Write PERL scripts to perform text parsing, data extraction, and report generation	2	3	2	2	3	1	-	L2,L3
C03	Develop TCL scripts to automate tool commands and control design processes in EDA tools.	3	3	3	2	3	-	-	L2,L3
C04	Construct Python scripts for file handling, data processing, and automation of design-related tasks.	2	3	2	3	3	2	3	L1,L4
C05	Compare the features of PERL, TCL, and Python, and select suitable scripting languages for specific EDA applications.	2	3	3	3	3	-	-	L4,L5

Syllabus:

UNIT-I

Introduction to Scripting Languages in EDA: Introduction to scripting and automation, Scriptingvs compiled languages, using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops– overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

UNIT- II

PERL Scripting: Scalar data, Arrays and list data, Hashes, Input and output, Control

structures, Regular expressions, Pattern matching with regex, Substitution and translation, using files and file handles, String manipulation, Subroutines, Using Perl modules, Command-line arguments and environment variables, Text parsing examples, Report generation

UNIT- III

TCL Scripting: Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, foreach), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation

UNIT-IV

Python for Design Automation and Data Processing: Python basics and data types, Expressions and operators, Flow control (if, for, while), Functions, Lists and dictionaries, String manipulation, File reading and writing, Pattern matching with regular expressions, Working with CSV and JSON files, Automating the keyboard and mouse, using os, sys, and subprocess modules, Writing utility scripts for automation

UNIT-V

Advanced Integration and Comparison: Comparison of PERL, TCL, and Python features, Strengths and weaknesses in EDA use-cases, best practices for automation and maintainability, calling external commands and shell integration in all three languages, Script interoperability usingintermediate files (CSV, JSON), Efficiency, readability, and debugging considerations, Choosing the right scripting language for given EDA tasks.

Self-Learning Topics: Resource sharing and priority inheritance protocols

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Approved in BOS No:01,08th September2025

Approved in ACM No: 01

TEXTBOOK:

1. Schwartz, Randal L., brian d foy, and Tom Phoenix. Learning Perl. 7th ed., O'Reilly Media,2016.
2. Welch, Brent B., Ken Jones, and Jeffrey Hobbs. Practical Programming in Tcl and Tk. 4th ed.,Prentice Hall, 2003.
3. Sweigart, Al. Automate the Boring Stuff with Python: Practical Programming for TotalBeginners. 2nd ed., No Starch Press, 2019.

REFERENCEBOOKS:

1. Robbins, Arnold. Scripting the UNIX System: Using Bash, Perl, and More. Addison-Wesley,2003.
2. Ousterhout, John K. Tcl and the Tk Toolkit. 2nd ed., Addison-Wesley Professional, 2009.
3. PythonSoftware Foundation. Python Language Reference Manual. https://docs.python.org.

Web References:

1. **https://www.researchgate.net/publication/320860067_Design_Automation_Using_Sc**

ript_Languages_High-Level
2. https://link.springer.com/book/10.1007/978-1-4757-1388-6
3. https://www.researchgate.net/publication/3893221_Scripting_for_EDA_tools_a_case_study

E-Books:

1. Design Automation, Languages, and Simulations (Chen**)**
2. Scripting Cultures (Burry)
3. LaSM – Solid Modeling Scripting

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- What is the purpose of scripting in design automation workflows?
- List any two advantages of using Python in automation.
- Define log file parsing in the context of scripting.
- What is meant by a GUI script?
- Name any two file handling commands in Tcl.
- Which scripting language is used extensively in Cadence design tools?

L2 – Understand

- Explain how scripting helps in parsing log files and timing reports during VLSI design.
- Interpret the importance of regular expressions (regex) in extracting data from simulation output files.
- Describe the use of GUI scripting in automating user interactions with EDA tools.
- Explain why scripting improves productivity and efficiency in large-scale design projects.
- Differentiate between shell scripting and EDA-specific scripting languages.

- How does automation with scripts reduce the chances of human error in chip design

L3 – Apply

- Develop a Python script to parse a timing report and extract all paths with negative slack.
- Apply regular expressions (regex) to extract only error messages from a large simulation log file.
- Write a shell script to automatically run multiple simulation testbenches one after another.
- Use Python matplotlib to plot a graph of power consumption vs. clock frequency from a given dataset.
- Create a Tcl procedure that takes two numbers as input and returns their greatest common divisor (GCD)

L4 – Analyze

- Analyze the trade-offs between using shell scripts vs. Python wrappers for invoking synthesis tools.
- Analyze their pros and cons in terms of portability and maintainability.
- Compare the efficiency of Tcl vs. Python for parsing large EDA tool reports.
- A Python script is failing to parse a log file because of incorrect regex usage.
- An EDA flow uses multiple nested shell scripts to run simulations.

L5 – Evaluate/Create

- Design a **Python-based framework** for parsing and analyzing multiple EDA timing reports.
- Evaluate the trade-offs between **Cadence SKILL** and **Python + APIs** for automating layout tasks.
- Design a **GUI tool (using Tcl-Tk or Python Tkinter)** that allows users to select input netlists and generate reports automatically.
- Create a **Python script** to integrate simulation results from multiple formats (CSV, TXT, XML) into a unified database.
- Design a **logging and error-handling mechanism** in Python for a large-scale regression automation system.

Chairperson

Board of Studies (ECE)

R25D57109 **CMOS DIGITAL IC DESIGN LAB** **0 0 4 2**

Course Objectives

1.Introduce CMOS Device Fundamentals
2. Develop CMOS Logic Design Skills
3.Understand Sequential Circuit Design
4.Analyze Performance Limitations due to Parasitics.
5.Promote Design Thinking and Simulation Practice

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
CO1	**Analyze** the static and dynamic characteristics of CMOS inverters, including switching threshold, noise margins, rise/fall times, and propagation delay.	3	2	1	1	1	-	-	L1, L3
CO2	**Design and simulate** basic CMOS combinational logic gates (NAND, NOR, AND) using static, pass-transistor, and dynamic logic styles and **compare** their performance in terms of delay, power, and area.	3	3	3	2	1	1	-	L3, L4
CO3	**Implement and verify** sequential circuits such as latches, flip-flops, and pipeline stages, and **evaluate** their timing behavior under clocked operation	3	3	2	2	2	-	2	L3, L4
CO4	**Differentiate** between custom transistor-level and standard cell design approaches for logic gates and arithmetic circuits, and **assess** trade-offs in layout, delay, and area.	3	3	3	2	3	2	3	L3, L4
CO5	**Examine** the effect of capacitive loading and interconnect parasitics (R, RC, RLC) on CMOS circuit delay, waveform distortion, and signal integrity	2	1	2	-	3	-	1	L2,L5

ListofExperiments: (Minimum 12 Experiments)

1.**Measure Voltage Transfer Characteristic (VTC) of CMOS Inverter**:Design a static CMOS inverter and plot the input vs. output voltage to determine switching threshold and noise margins.
2. **Determine Propagation Delay of CMOS Inverter**:Apply a square wave input, simulate the output waveform, and measure the rise time, fall time, and propagation delay.
3. **Design and Simulate CMOS NAND Gate**:Implement a 2-input NAND gate using CMOS and verify its truth table and transient response.
4. **Compare Static CMOS and Pass-Transistor NAND Gate**:Design both logic styles for NAND gate, simulate output voltage levels, and compare delay and power.
5. **Design a Dynamic CMOS NOR Gate**:Create a dynamic NOR gate, simulate precharge and evaluation phases, and observe output waveform timing.
6. **Implement and Simulate a Static SR Latch**:Design an SR latch using CMOS transistors; verify bistability by applying input set/reset sequences.

7. **Design a Master-Slave D Flip-Flop**:Build a master-slave edge-triggered flip-flop, apply clock and data inputs, and verify timing and output behavior.
8. **Compare Latch-Based and Register-Based Pipeline Stages**:Design a simple 2-stage pipeline using latches and registers; simulate and compare data propagation delays.
9. **Custom vs Standard Cell Design of a 2-Input AND Gate**:Implement a 2-input AND gate using full custom transistor-level design and standard cell approach; compare layout area.
10. **Array-Based Implementation of a 2-Bit Adder**:Design a 2-bit adder using an array-based logic style; simulate functional correctness and evaluate area.
11. **Analyze Delay Due to Capacitive Load on CMOS Inverter**:Add different load capacitances to inverter output and simulate the resulting delay variation.
12. **Effect of Interconnect Resistance on Signal Propagation**:Model a resistive interconnect connected to a CMOS inverter output; simulate delay and signal attenuation.
13. **Simulate Interconnect RC Parasites Impact on Output Waveform**:Extract parasitic RC values for a simple wire segment and simulate their effect on signal rise and fall times.
14. **Compare Signal Integrity with and without Interconnect Inductance**: Model a simple interconnect with inductance; simulate signal ringing and delay effects compared to purely RC models.

Board of Studies: Electronics and Communication Engineering
Approved in BOS No:01, 08th September2025
Approved in ACM No: 01

Web References

- NPTEL – https://digitaldesign/108/105/108105158/
- Tutorials: https://www.electronics-tutorials.ws/
- All About Circuits: https://www.allaboutcircuits.com/
- https://www.cmos inverter similation 4u.com/
- Virtual Labs – https://vlab.amrita with plds.edu/

E-Books

- Digital Integrated Circuit Design: A Design Perspective (Rabaey)
- Digital Integrated Circuit Design From VLSI Architectures to CMOS Fabrication
- CMOS Circuit Design, Layout, and Simulation (3rd Edition)

Internal Assessment Pattern Sample

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	10%	5%
L2	20%	15%
L3	40%	40%
L4	30%	40%
L5	—	—
Total (%)	**100**	**100**

Questions by Cognitive Level

L1 – Recall (Short Answer)

1. Define Voltage Transfer Characteristic (VTC) of a CMOS inverter.
2. List the parameters used to measure propagation delay in CMOS inverters.
3. State the difference between static CMOS and dynamic CMOS logic.
4. What is the function of a D flip-flop?
5. Define parasitic capacitance and resistance in interconnects

L2 – Understand (SA/LA)

1. Explain how the switching threshold of a CMOS inverter is determined from the VTC.
2. Describe the role of precharge and evaluation phases in dynamic CMOS NOR gates.
3. Differentiate between latch-based and register-based pipeline stages.
4. Explain how interconnect resistance affects signal integrity in CMOS circuits.
5. Summarize the advantages of using current mirrors in digital IC design.

L3 – Apply (LA)

1. Design a CMOS NAND gate and verify its truth table through simulation.
2. Apply capacitive loads to an inverter output and measure the effect on delay.
3. Implement a static SR latch using CMOS and test its bistability.
4. Build a master–slave flip-flop and verify timing behavior using a test clock.
5. Simulate a 2-bit array-based adder and verify functionality with input combinations.

L4 – Analyze (LA)

1. Analyze the rise and fall times in a CMOS inverter under different load capacitances.
2. Compare delay and power consumption between static CMOS NAND and pass-transistor NAND gates.
3. Examine the impact of interconnect RC parasitics on output waveform shape.
4. Distinguish between custom transistor-level design and standard-cell design for a 2-input AND gate.
5. Investigate noise margins of CMOS inverters and justify their significance.

L5 – Evaluating (LA)

1. Evaluate the performance of a CMOS dynamic NOR gate versus its static counterpart.
2. Assess the effect of interconnect inductance on signal ringing and waveform distortion.
3. Judge which design (latch-based or register-based pipeline) is more efficient in terms of delay and power.
4. Critique the area and speed trade-offs in array-based vs full-custom adder design.
5. Validate simulation results of propagation delay with theoretical calculations.

Chairperson

Board of Studies (ECE

R25D57110 CMOS ANALOG IC DESIGN LAB 0 0 4 2

Course Objectives

1.Understand MOS Device Behavior
2. Develop Modeling and Simulation Skills
3.Design and Analyze Basic Amplifier Configurations
4.Explore Differential and Multistage Circuits.
5.Design Complex Analog Systems

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
CO1	Design and simulate MOS transistors to analyse their electrical characteristics and model parameters.	3	2	1	1	1	-	-	L1, L3
CO2	Implement and evaluate single-stage amplifiers including common-source, source follower, and common-gate configurations.	3	3	3	2	1	1	-	L3, L4
CO3	Design differential amplifiers with resistive and active loads and measure their gain and common-mode rejection properties.	3	3	2	2	2	-	2	L3, L4
CO4	Develop basic, cascode, and active current mirrors, analyzing their current replication and output impedance.	3	3	3	2	3	2	3	L3, L4
CO5	Design and analyse two-stage CMOS operational amplifiers focusing on gain, stability, and frequency response.	2	1	2	-	3	-	1	L2,L5

ListofExperiments: (Minimum 12 Experiments)

1.**MOSFET I-V Characteristics Simulation**: Design and simulate NMOS and PMOS transistors to plot ID vs VDS and ID vs VGS characteristics; analyze threshold voltage and saturation behavior.
2.**Effect of Second-Order Parameters on MOS Device Performance**: Simulate and study effects like channel length modulation, body effect, and velocity saturation on transistor I-V characteristics.
3.**Extraction of MOS Device Model Parameters Using SPICE**: Extract and verify MOSFET parameters (threshold voltage, mobility, etc.) from device simulation for different model levels.
4.**Design and Simulation of Common-Source Amplifier with Resistive Load**: Design a common-source amplifier and analyze voltage gain, input/output impedance, and frequency response.
5.**Design and Simulation of Common-Source Amplifier with Diode-Connected Load**: Implement a CS amplifier with diode-connected load and compare gain and linearity with resistive-load version.
6.**Design and Analysis of Source Follower (Common-Drain) Amplifier**: Build a source follower circuit; simulate and measure voltage gain, output impedance, and linearity.
7.**Design and Simulation of Common-Gate Amplifier**: Design a common-gate stage and analyze its input/output characteristics and high-frequency response.

8.**Design of Basic Differential Pair with Resistive Load**: Simulate a differential pair and analyze differential gain, common-mode gain, and calculate CMRR.
9.**Differential Amplifier with MOS Current Mirror Load**: Implement a differential pair with active current mirror load; analyze improvements in gain and CMRR.
10.**Simulation of Gilbert Cell Mixer**: Design a Gilbert cell circuit and simulate frequency mixing operation with two sinusoidal inputs.
11.**Design and Simulation of Basic Current Mirror**: Implement a basic current mirror; simulate output current accuracy and dependence on transistor sizing.
12.**Design and Simulation of Cascode Current Mirror**: Build a cascode current mirror; analyze output impedance and current matching improvement.
13. Design of Active Current Mirror Circuits: Implement Wilson or improved current mirrors; simulate and compare performance with basic and cascode types.
14. Design and Simulation of Two-Stage CMOS Operational Amplifier: Design a two-stage op-amp; analyze gain, phase margin, unity gain bandwidth, and frequency response.

Board of Studies: Electronics and Communication Engineering
Approved in BOS No:01, 08th September2025
Approved in ACM No: 01

Web References

- NPTEL – https://cmos analog ic design/108/105/108105158/
- Tutorials: https://www.electronics-tutorials.ws/
- All About Circuits: https://www.allaboutcircuits.com/
- https://www.operational similation 4u.com/
- Virtual Labs – https://vlab.amrita with plds.edu/

E-Books

- Design of Analog CMOS Integrated Circuits (Behzad Razavi)
- CMOS Analog Circuit Design (Allen & Holberg, 3rd Edition)
- CMOS Circuit Design, Layout, and Simulation (3rd Edition)

Internal Assessment Pattern Sample

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	10%	5%
L2	20%	15%
L3	40%	40%
L4	30%	40%
L5	—	—
Total (%)	**100**	**100**

Questions by Cognitive Level

L1 – Recall (Short Answer)

1. Define threshold voltage of a MOSFET.

2. List the different regions of operation of a MOS transistor.
3. State the function of a common-source amplifier.
4. What is CMRR in a differential amplifier?
5. Mention two advantages of cascode current mirror

L2 – Understand (SA/LA)

1. Explain the effect of channel length modulation on MOSFET I–V characteristics.
2. Describe the difference between CS amplifier with resistive load and diode-connected load.
3. Explain the role of body effect in MOS transistor behavior.
4. Illustrate why source follower has unity gain.
5. Explain how current mirrors improve differential amplifier gain and CMRR.

L3 – Apply (LA)

1. Simulate **ID-VDS** characteristics of NMOS and extract threshold voltage.
2. Apply SPICE to study the velocity saturation effect in short-channel MOSFETs.
3. Implement a source follower and measure its input and output impedance.
4. Simulate a basic current mirror and verify output current matching.
5. Apply a Gilbert Cell Mixer design to show frequency translation between LO and RF.

L4 – Analyze (LA)

1. Compare gain and linearity of CS amplifier& resistive load and diode-connected load.
2. Analyze the trade-off between output swing and gain in a CS amplifier.
3. Differentiate between diff pair with resistive load and current mirror load.
4. Compare the output impedance of basic, cascode, and Wilson current mirrors.
5. Analyze the frequency response of CG vs CS amplifier.

L5 – Evaluating (LA)

1. Evaluate which MOS amplifier topology (CS, CG, CD) is best suited for high-frequency applications.
2. Assess the accuracy of SPICE Level-1 and Level-3 MOS models for device simulation.
3. Justify the use of Gilbert Cell Mixer in RF applications compared to other mixers.
4. Judge the stability of a two-stage CMOS op-amp using phase margin and gain margin.
5. Critique the trade-off between current mirror accuracy and voltage headroom.

Chairperson

Board of Studies (ECE)

R25MBA101 **Research Methodology & IPR** **2 0 0 2**

(M. Tech Computer Science and Engineering)

Course Objectives:

1. To understand the research problem
2. To know the literature studies, plagiarism and ethics
3. To get the knowledge about technical writing
4. To analyze the nature of intellectual property rights and new developments
5. To know the patent rights

Course Outcomes: At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasise the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

SYLLABUS

UNIT-I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT-II

Effective literature studies approaches, analysis, Plagiarism, Research ethics.

UNIT-III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT-IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students"

2. C.R. Kothari, Research Methodology, methods & techniques, 2nd edition, new age International publishers.

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"

2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

3. Mayall, "Industrial Design", McGraw Hill, 1992.

Chairperson
Board of Studies (MBA)

R25BS101 20 0 0

ENGLISHFORRESEARCHPAPERWRITING

(Audit-I&II .1)

Pre-requisite:None

Courseo bjectives:

- To Understand that how to improve your writing skills and level of readability
- To Learn about what to write in each section
- To Understand the skills needed when writing a Title Ensure the good quality of paper at very First-time submission

1. **Introduction to Research**
   - Definition, purpose, and importance of research; Types of research:Basicvs. applied,quantitativevs.qualitative;Stages:Problemidentification, literature review, design, data collection, analysis, reporting; Structure, objectives, methodology, timeline, budget;
2. **Formulating Research Questions and Hypotheses**
   - Characteristicsofgoodresearchquestions;Hypothesistypesandformulation
3. **Literature Review**
   - Purpose,process, andtools(e.g.,databases, SCIMAGOandgoogle scholar, etc.)
4. **Research Design**
   - Tools of data collection; Data collection through Surveys, questionnaires, experiments, structured observations; Interviews, focusgroups,ethno graphy, content analysis; types of research - Exploratory, descriptive, explanatory, experimental; Cross-sectional vs. longitudinal studies;
   - Sample size considerations;
5. **Ethics in Research**
   - Informed consent, confidentiality, research with vulnerable populations; Institutional Review Boards(IRBs);plagiarism and how to avoid plagrism; Proper citation and referencing

Publishing and Disseminating Research:

- Journals,conferences, researchreports; Peerreview process

TEXT BOOK/REFERENCES:

1. GoldbortR(2006)WritingforScience,YaleUniversityPress(availableonGoogleBooks)
2. DayR(2006) HowtoWriteandPublishaScientificPaper,CambridgeUniversityPress
3. HighmanN(1998),Handbook ofWritingfortheMathematicalSciences,SIAM.Highman's book
4. AdrianWallwork,EnglishforWritingResearchPapers,SpringerNewYorkDordrec htHeidelberg London, 2011

Chairperson
Board of Studies(ENGLISH)

R25BS102 **DISASTERMANAGEMENT** **1 0 0 1**

(Common to all P.G course)

Course Objectives:

1. To learn to demonstrate a critical understanding of key conceptsin disaster risk reduction and humanitarian response.
2. To evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Todevelopanunderstandingofstandardsofhumanitarianresponseand practical relevance in specific types of disasters and conflict situations.
4. Tounderstandthestrengthsandweaknessesofdisastermanagementapproaches,
5. To plan and program in different countries, particularly their home country or thecountries they work

SYLLABUS

UNIT-I

Introduction: Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT-II

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Land slides and Avalanches, Man-made disaster: NuclearReactorMeltdown, Industrial Accidents, Oil Slicks and Spills, Out breaks of Disease and
Epidemics, War and Conflicts.

UNIT-III

DisasterProneAreasin India:StudyofSeismic Zones; AreasPronetoFloodsandDroughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

UNIT-IV

DisasterPreparednessand Management: Preparedness: Monitoring ofPhenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-V

Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People’s Participation In Risk Assessment. Strategies for Survival.

UNIT-VI

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXTBOOKS/REFERENCES:

1. R. Nishith, Singh AK, "Disaster Managementin India: Perspectives, issues and strategies "'New Royal book Company.

2. Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesandReflections", Prentice Hall Of India, New Delhi.

3. GoelS.L.,DisasterAdministrationandManagementTextandCaseStudies", Deep & Deep Publication Pvt. Ltd., New Delhi.

Chairperson
Board ofStudies(Chemistry)

R25D57201**MIXED SIGNAL IC DESIGN (PE - III)**3 0 0 3

Course Objectives:

1. To design and analyze mixed-signal integrated circuits.
2. To analyze and design switched-capacitor circuits.
3. To model analog and mixed-signal components using Verilog and Verilog
4. To design digital-to-analog and analog-to-digital converter circuits.
5. To Design of frequency and Q tunable continuous time filters

Course Outcomes

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Analyse sinusoidal signals and frequency-domain representations using Fourier tools and transformmethods.	3	3	1	1	1	-	-	L1,L2
C02	Evaluate the effects of sampling, aliasing, and interpolation on analog signals and implementsample-and-hold circuits.	3	3	2	2	1	-	-	L2,L3
C03	Design analog filters using active-RC, MOSFET-C, and gm-C topologies and interpretdiscrete-time filtering behaviour	2	3	3	2	1	-	-	L2,L3
C04	Implement basic digital filters using FIR/IIR techniques and evaluate performance usingDAC/ADC SPICE models.	3	3	2	3	2	-	-	L4
C05	Assess the performance of data converters based on quantization noise, SNR, and apply noiseshapingmethods to improve resolution.	1	3	3	2	3	-	-	L4,L5

Syllabus:

UNIT - I

Signals, Filters and Tools: Sinusoidal signals, in-phase and quadrature signals, the complex (z-)plane, comb filters – the digital comb filter, the digital differentiator, the digital integrator, representing signals – exponential Fourier series, Fourier transform, Dirac Delta function.

UNIT - II

Sampling and Aliasing: Sampling – impulse sampling, decimation, the sample-and-hold (S/H), S/H spectral response, the reconstruction filter (RCF), circuit concerns for implementing the S/H, interpolation, Zero padding, Hold register, linear interpolation, K-path sampling – switched capacitor circuits, non-overlapping clock generation, implementing the S/H, the S/H with gain.

UNIT - III

Analog Filters: Integrator building blocks – low pass filters, active-RC integrators, MOSFET-C integrators, gm-C (transconductance-C) integrators, discrete-time integrators, filtering topologies –the bilinear transfer function, the bquadratic transfer function

UNIT - IV

Digital Filters – SPICE models for DACs and ADCs, the ideal DAC, the ideal ADC, Sinc-shaped digital filters, band pass and high pass Sinc filters, interpolation using Sinc filters, filtering topologies – FIR filters, the bilinear transfer function, the bilinear transfer function

UNIT – V

Data Converters: Quantization noise, signal-to-noise ratio (SNR), clock jitter, improving SNR using averaging, the one-bit ADC and DAC, passive noise-shaping, improving SNR and linearity.

Self-Learning Topics: Built-In Self-Test (BIST) techniques for mixed-signal ICs.

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01, 08th September2025

Approved in ACM No: 01

TEXT BOOK:

1. R. Jacob Baker, CMOS Mixed-Signal Circuit Design, Second Edition, Wiley–IEEE Press,2008.
2. David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 1997.

REFERENCE BOOKS:

1. Razavi, Behzad. Design of Analog CMOS Integrated Circuits. 2nd ed., McGraw-Hill Education, 2017.
3. Johns, David A., and Ken Martin. Analog Integrated Circuit Design. Wiley, 1997.
4. Sansen, Willy M.C. Analog Design Essentials. Springer, 2006.
5. Allen, Phillip E., and Douglas

Web References:

1. **https://mixedsignal.wordpress.com/**
2. **https://www.researchgate.net/**
3. **https://link.springer.com/book/10.1007/978-1-4419-6478-6**

eBooks:

1. Mixed-Signal Systems: A Guide to CMOS Circuit Design.
2. CMOS: Mixed-Signal Circuit Design, Second Edition — R. Jacob Baker (Wiley)
3. Extreme Low-Power Mixed Signal IC Design — A. Tajalli (Springer)

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Expand the abbreviations **ADC** and **DAC**.
- State the function of a **Phase-Locked Loop (PLL)**.
- List any two applications of **mixed-signal ICs**.
- What is the difference between **analog** and **digital** signals?

- Name two **CMOS devices** used in mixed-signal design.
- What is the function of a **sample-and-hold circuit**?

L2 – Understand

- Explain the difference between analog, digital, and mixed-signal circuits with examples.
- Explain how an ADC converts an analog signal into a digital form.
- Compare the working of a Flash ADC and a Successive Approximation Register (SAR) ADC.
- Describe the role of a DAC in audio signal processing.
- Explain why CMOS technology is widely used in mixed-signal IC design.
- Interpret the importance of linearity in data converters.

L3 – Apply

- Apply the FFT method to measure the SNR of an ADC given a sampled output waveform.
- Design a simple DAC resistor ladder for a 3-bit digital input.
- Apply layout isolation techniques to suggest methods for reducing noise coupling between analog and digital blocks.
- Design a simple RC low-pass filter for anti-aliasing with a cutoff frequency of 1 kHz.
- Use oversampling to improve resolution: How many times oversampling is required to gain an extra 2 bits of resolution.

L4 – Analyze

- Analyze the trade-offs between a Flash ADC and a SAR ADC in terms of speed, area, and power.
- Compare the linearity and speed of R-2R ladder DAC vs. Current-Steering DAC.
- Analyze the effect of clock jitter on high-speed ADCs.
- Compare time-domain vs. frequency-domain testing of mixed-signal ICs.
- Analyze why mixed-signal IC testing is more challenging compared to digital IC testing.

L5 – Evaluate/Create

- Design a **10-bit, 1 MS/s ADC** architecture suitable for a low-power IoT device and justify your choice.
- Evaluate whether a **Flash ADC** or **Sigma-Delta ADC** is more suitable for biomedical applications (e.g., ECG monitoring).
- Propose a **mixed-signal system-on-chip (SoC)** architecture that integrates sensors, ADC/DAC, and a microcontroller.
- Justify the selection of **CMOS technology** for implementing a mixed-signal IC compared to BiCMOS.
- Design a **low-power DAC** for portable audio applications and evaluate its trade-offs in resolution vs. power.

Chairperson
Board of Studies (ECE)

R25D57202**FPGA BASED SYSTEM DESIGN (PE - IV)**3 0 0 3

Course Objectives:

1. To Evolution and Basics of ICs and Digital System Design.
2. To ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.
3. To Verilog Coding and Simulation of Digital Systems using Xilinx
4. To Implementation of Digital circuits in FPGA processor.
5. To Implement digital circuits in Xilinx FPGA processor using Hardware description Language experimentally.

Course Outcomes

CourseCode	Course Outcomes	MappingwithPOs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Explain the architectural features and functional components of FPGA-based systems anddescribe their advantages in digital design applications.	3	2	1	1	2	-	-	L1,L2
C02	Design combinational logic circuits using Verilog HDL and evaluate them for delay, power, and resource utilization on FPGA platforms.	3	2	2	2	2	-	-	L2,L3
C03	Develop and simulate sequential logic circuits and finite state machines using appropriatedesign styles and clocking rules.	2	3	3	2	3	-	-	L2,L3
C04	Apply behavioural design methodologies and demonstrate system modelling using HDLs in real-worldcase studies.	2	3	2	3	2	-	-	L4
C05	Analyse and propose solutions for large-scale FPGA-based systems involving busses, platformFPGAs, and multi-FPGA architectures	2	2	3	2	3	-	-	L4,L5

Syllabus:

UNIT - I

Introduction to FPGA-Based Systems: Introduction, basic concepts, digital design and FPGAs,FPGA-based system design, FPGA architectures, SRAM-based FPGAs, permanently programmed FPGAs, chip I/O, circuit design of FPGA fabrics, architecture of FPGA fabrics.

UNIT - II

Combinational Logic Design in FPGAs: Introduction, the logic design process, hardware description languages -modelling with HDLs, Verilog, Combinational network delay, power and energy optimization, arithmetic logic, logic implementation for FPGAs, physical design for FPGAs, the logic design process revisited.

UNIT - III

Sequential Logic and State Machines: Introduction, the sequential machine design process, sequential design styles, rules for clocking, performance analysis, power optimization

UNIT - IV

Design Methodologies and Behavioural Architecture: Introduction, behavioural design, design methodologies, design example

UNIT – V

System-Level Design and Advanced FPGA Applications: Introduction, buses, platform FPGAs, multi-FPGA systems, Novel architectures.

Self-Learning Topics: logic implementation for FPGAs, physical design for FPGAs

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01, 08th September2025

Approved in ACM No: 01

TEXT BOOK:

1. Wolf, Wayne. FPGA-Based System Design. Pearson Education India, 2005..

REFERENCE BOOKS:

1. Maxfield, Clive. The Design Warrior's Guide to FPGAs: Devices, Tools and Flows. Newnes,1st ed., 2004.
2. Trimberger, Stephen M. Field-Programmable Gate Array Technology. Springer Science &Business Media, 2012.
3. Kuon, Ian, Russell Tessier, and Jonathan Rose. FPGA Architecture: Survey and Challenges.

Web References:

1. https://www.tce.edu/tce-mooc/fpga-based-digital-system-design
2. https://www.coursera.org/specializations/fpga-design
3. https://www.google.com/search?q=FPGA+BASED+SYSTEM+DESIGN

eBooks:

1. Advanced Digital System Design – A Practical Guide to Verilog-Based FPGA and ASIC Implementation (Shirshendu Roy, 2024).
2. Advanced Digital System Design Using SoC FPGAs: An Integrated Hardware/Software Approach (Ross K. Snider, 2023)
3. Introduction to Embedded System Design Using Field Programmable Gate Arrays (Rahul Dubey, 2009)

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Expand **VHDL** and **Verilog**.
- Define **synthesis** in FPGA design flow.
- What is the role of **I/O blocks** in FPGA architecture?
- Write any two advantages of **FPGA over microcontrollers**.

- Define **reconfigurability** in FPGA context.

L2 – Understand

- Explain the role of Configurable Logic Blocks (CLBs), I/O Blocks (IOBs), and Interconnects in an FPGA.
- Why are Look-Up Tables (LUTs) considering the fundamental building blocks in FPGA design?
- Compare hard-core vs. soft-core processors in FPGA-based systems.
- Explain the FPGA design flow from HDL coding to device programming.
- Describe the importance of reconfigurability in FPGA-based systems.
- Why is FPGA preferred for rapid prototyping compared to ASICs?

L3 – Apply

- Write a **Verilog/VHDL code snippet** to implement a 4:1 multiplexer on an FPGA.
- Apply the FPGA design flow to describe the steps needed to implement a **digital FIR filter**.
- Design a **counter** that counts from 0 to 9 and resets back to 0, using Verilog/VHDL.
- An FPGA has **4-input LUTs**. How many configuration bits are needed per LUT?
- Implement a **4-bit synchronous up-counter** in Verilog/VHDL and explain its mapping to FPGA resources.

L4 – Analyze

- Analyse the **trade-offs between FPGA and ASIC** in terms of speed, cost, and flexibility.
- A Verilog design **synthesizes correctly but fails in simulation**. Analyse possible causes.
- Compare **behavioural vs. structural modelling** in HDL design and their impact on FPGA synthesis.
- Analyse the effect of **timing violations** in FPGA implementation. What could be the reasons and fixes?
- Compare the performance of a **hard-core processor** vs. a **soft-core processor** implemented on an FPGA.

L5 – Evaluate/Create

- Design an **FPGA-based image processing system** (e.g., edge detection). Justify your choice of FPGA resources (LUTs, DSPs, BRAM).
- Evaluate the suitability of **FPGA vs. GPU** for real-time signal processing applications.
- Propose an **FPGA architecture for an IoT edge device** including ADC, processor, and wireless interface.
- Design a **system-on-chip (SoC)** on an FPGA that integrates a soft-core CPU, memory, and peripherals.
- Propose an **FPGA-based accelerator** for matrix multiplication and justify its efficiency over a CPU-based solution.

Chairperson
Board of Studies (ECE)

R25D57203 VLSI Test and Testability 3 0 0 3

Course Objectives:

1. Introduce the fundamentals of VLSI testing, including fault models, design errors, and test quality metrics.
2. Familiarize students with design-for-testability (DFT) principles such as scan design, boundary scan, BIST (Built-In Self-Test), and test compression.
3. Study different low power design methodologies at circuit, logic, architectural, and system levels.
4. Develop understanding of memory testing strategies, including March tests, redundancy techniques, and repair methodologies.
5. Explore CAD tools and methodologies for low power VLSI design.

Course Outcomes

CourseCode	Course Outcomes	MappingwithPOs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Identify different types of faults in digital circuits and explain their corresponding logical fault models.	3	3	2	2	1	-	-	L1,L2
C02	Apply test generation techniques to detect faults in combinational and sequential digital circuits.	3	3	3	2	1	-	-	L2,L3
C03	Design scan-based and ad-hoc DFT archi-tectures for improving circuit testability.	3	3	3	2	2	-	-	L2,L3
C04	Implement Built-In Self-Test (BIST) strate-gies for digital systems and memory blocks.	3	3	3	3	2	-	-	L2,L3
C05	Analyse fault diagnosis techniques to locate and interpret faults in logic-level digital circuits.	3	3	2	2	2	-	-	L1,L2

Syllabus:

Unit-I:

Basics of Testing and Fault Modeling: Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

Unit-II:

Test Generation for Combinational and Sequential Circuits: Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. Design For Testability

Unit-III:

Design for Testability: Ad-hoc design - Generic scan-based design - Classical scan-based design –System level DFT approaches**.**

Unit-IV:

Self-Test and Test Algorithms: Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

Unit-V:

Fault Diagnosis:Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking

Board of Studies: Electronics and Communication Engineering
Approved in BOS No:01, 08th September2025
Approved in ACM No: 01

Text Books

1. Abramovici, M., M. A. Breuer, and A. D. Friedman. Digital Systems Testing and Testable
Design. 1st ed., Jaico Publishing House, 2002.

2. Bushnell, M. L., and V. D. Agrawal. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits. Illustrated ed., Springer Science & Business Media, 2006

Reference Books

1. Lala, P. K. Digital Circuit Testing and Testability. Academic Press, 2002.

2. Crouch, A. L. Design-for-Test for Digital IC's and Embedded Core Systems. 1st ed., Prentice Hall International, 1999

Web References:

1. https://www.tutorialspoint.com/vlsi_design/vlsi_design_low_power.htm
2. https://vlsiuniverse.blogspot.com/2013/01/sources-of-power-dissipation-in-cmos.html
3. https://www.geeksforgeeks.org/low-power-vlsi-design-techniques
4. https://nptel.ac.in/courses/106/105/106105161
5. https://www.ibm.com/internet-of-things

eBooks:

1. VLSI Test Principles and Architectures: Design for Testability — Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen.
2. VLSI Testing & Testability — Course Material (Scribd).

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define power dissipation in CMOS circuits.

- List the different sources of power consumption in digital VLSI circuits.
- What is static power dissipation?
- What is dynamic power dissipation?
- List any two techniques to reduce leakage current in submicron technologies.

L2 – Understand

- Explain why low power design is critical in modern VLSI circuits.
- Describe the difference between static power and dynamic power dissipation.
- Explain how switching activity affects power consumption in CMOS circuits.
- Summarize the role of power estimation techniques in VLSI design.
- Explain the impact of supply voltage scaling on power and performance.

L3 – Apply

- Apply power estimation techniques to calculate the energy consumption of a given CMOS inverter chain.
- Design a 4-bit adder with clock gating and compare its power usage with a conventional design.
- Use supply voltage scaling to analyze the effect on delay and power in a simple combinational logic circuit.
- Apply MTCMOS techniques to a sequential circuit to reduce leakage power.
- Implement a low-power multiplexer using transistor-level optimizations and measure power reduction.

L4 – Analyze

- Analyze the dynamic vs. static power consumption in a CMOS circuit and identify which dominates at different technology nodes.
- Compare the effectiveness of clock gating and power gating for reducing overall power.
- Analyze the impact of threshold voltage scaling (Vth scaling) on leakage and performance.
- Differentiate between multi-Vdd and dynamic voltage scaling (DVS) approaches for power reduction.
- Analyze the trade-offs between low power design and circuit performance in submicron technologies.

L5 – Evaluate/Create

- Evaluate different low-power design methodologies and recommend the most suitable one for battery-powered IoT devices.
- Critically analyze the trade-offs among power, performance, and area (PPA) in a given VLSI design.
- Evaluate the effectiveness of multi-threshold CMOS (MTCMOS) compared to power gating for leakage reduction.
- Justify the choice of supply voltage scaling for ultra-low-power applications, considering performance constraints.
- Recommend the best low-power optimization technique for mobile processors and justify your reasoning.

Chairperson

Board of Studies (ECE)

R25D57204PHYSICAL DESIGN AUTOMATION WITH AI3 0 0 3

Course Objectives:

1. Introduce the fundamentals of VLSI physical design automation, including floorplanning, placement, routing, clock tree synthesis, and optimization.
2. Explain the limitations of traditional physical design automation tools and motivate the need for AI-driven approaches.
3. Familiarize students with AI/ML algorithms (supervised, unsupervised, and reinforcement learning) relevant to EDA and physical design.
4. Develop understanding of data-driven optimization techniques for placement, routing, congestion management, timing closure, and power reduction.
5. Expose learners to AI-based frameworks and tools used in next-generation design automation flows.

Course Outcomes

CourseCode	Course Outcomes		MappingwithPOs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Explain the physical design flow in VLSI and apply basic graph algorithms used in EDA tools.	3	2	2	1	-	-	-	L1,L2
C02	Demonstrate understanding of chip plan-ing techniques including floorplanning, placement,and routing.	3	3	2	2	1	-	-	L2,L3
C03	Analyze and implement routing strategies and clock tree synthesis for efficient signal distribution.	3	3	3	2	1	-	-	L2,L3
C04	Evaluate timing closure techniques to ensure performance and reliability in VLSI designs.	3	3	3	3	2	1	-	L2,L3
C05	Identify and discuss the applications and limitations of machine learning in physical design automation.	3	2	2	2	1	-	-	L1,L2

Syllabus:

Unit I:

Introduction to Physical Design and AI in EDA: Introduction - Electronic Design Automation (EDA), VLSI Design Flow, VLSI Design Styles, Layout Layers and Design Rules, Physical Design optimizations, Algorithms and Complexity, Graph Theory Terminology, Common EDA Terminology. Netlist and System Partitioning– Introduction, KL and FM Algorithms, Multilevel Partitioning.

Unit-II:

Chip Planning and Placement: Introduction, optimization goals, floorplan representations, floorplanning algorithms, pin assignment, power and ground routing. Global placement, legalization and detailed placement

Unit-III: Routing and Clock Tree Synthesis: Introduction, optimization goals, representations of routing regions, the global routing flow, single-net and full-net routing,

detailed routing – horizontal and vertical nstraint graphs, channel and switchbox routing, area routing, clock routing, modern clock tree synthesis.

Unit – IV:

Timing Closure: Timing analysis, and performance constraints, timing-driven placement, timing driven routing, physical synthesis, performance-driven design flow.

Unit-V:

Machine Learning in Physical Design: Introduction ML promises and challenges in physical design, Canonical ML applications, the state of ML for physical design.

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01,08th September2025

Approved in ACM No: 01

Text Book

1. Kahng, Andrew B., et al. VLSI Physical Design: From Graph Partitioning to Timing Closure. 2nd ed., Springer International Publishing, 2022.

2. Sherwani, Naveed A. Algorithms for VLSI Physical Design Automation. 3rd ed., Springer, 2012.

Reference Books

1. Hsiao, Michael. Machine Learning Applications in Electronic Design Automation.Morgan & Claypool, 2020.

2. Cong, Jason, and Bei Yu. Machine Learning and AI for EDA: From Fundamentals to Advanced Applications. Springer, 2022.

Web References:

1. https://vlsiuniverse.blogspot.com/2013/04/vlsi-physical-design-flow.html
2. https://www.synopsys.com/implementation-and-signoff.html
3. https://ieee-ceda.org/publications/ieee-design-test/ai-machine-learning-eda
4. https://nptel.ac.in/courses/106/105/106105161
5. https://www.researchgate.net/publication/356900717_Machine_Learning_in_VLSI_Physical_Design_Automation

eBooks:

1. Algorithms for VLSI Physical Design Automation — Naveed A. Sherwani (3rd Edition).
2. Handbook of Algorithms for Physical Design Automation

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define physical design automation in VLSI.
- List the main phases of physical design flow (floorplanning, placement, routing, etc.).

- What is floorplanning and why is it important in chip design?
- Recall the types of routing used in VLSI physical design.
- State the role of clock tree synthesis (CTS) in physical design.

L2 – Understand

- Explain the steps involved in the VLSI physical design flow with examples.
- Differentiate between floorplanning and placement in chip design.
- Illustrate how clock tree synthesis (CTS) affects timing and power in physical design.
- Summarize the importance of routing strategies in ensuring signal integrity.
- Explain why timing closure is a critical step in VLSI design.

L3 – Apply

- Apply a graph partitioning algorithm to divide a netlist into sub-blocks for floorplanning.
- Given a chip area and module sizes, create a simple floorplan that minimizes wirelength.
- Use Dijkstra□s shortest path algorithm to find an optimal routing path for a given net.
- Implement a basic clock tree structure to distribute the clock signal uniformly across flip-flops.
- Apply timing analysis techniques to verify whether a given circuit meets the required setup time.

L4 – Analyze

- Analyze the impact of floorplanning decisions on wirelength, congestion, and timing closure.
- Compare different placement algorithms (e.g., simulated annealing vs. min-cut partitioning) and discuss their trade-offs.
- Examine a routing congestion map and identify the critical regions affecting performance.
- Analyze how clock tree synthesis (CTS) variations influence skew and power consumption.
- Compare traditional optimization methods with AI-driven placement or routing approaches in terms of quality and runtime.

L5 – Evaluate/Create

- Design a complete AI-assisted placement and routing workflow for a given SoCnetlist. Justify your algorithm choices.
- Propose a reinforcement learning model to optimize congestion reduction and timing closure simultaneously. Evaluate its expected benefits over traditional methods.
- Create a hybrid AI-traditional algorithm for clock tree synthesis that balances skew and power consumption.
- Evaluate multiple AI-based floorplanning strategies for a given chip and select the most effective one based on PPA metrics.
- Design a machine learning model to predict post-placement wirelength and routing congestion for large-scale designs.

Chairperson

Board of Studies (ECE)

R25D57205Functional Verification using SystemVerilog and UVM3 0 0 3

Course Objectives:

1. Introduce SystemVerilog constructs and methodologies for building scalable and reusable testbenches.
2. Develop skills in advanced verification techniques, including constrained random stimulus generation and functional coverage.
3. Familiarize students with Assertion-Based Verification (ABV) and its role in improving design quality and bug detection.
4. Provide hands-on experience with Universal Verification Methodology (UVM) to design modular, reusable, and configurable verification environments.
5. Enable students to implement coverage-driven verification (CDV) strategies for effective validation of complex digital designs.

Course Outcomes

Course Code	Course Outcomes		MappingwithPOs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Write basic SystemVerilog testbenches using data types, control statements, and functions.	3	3	2	2	1	-	-	L1,L2
C02	Use object-oriented programming and randomization to create flexible and reus-able testbenches.	3	3	3	2	1	-	-	L2,L3
C03	Measure verification quality using functi-onal coverage in SystemVerilog.	3	3	3	2	2	-	-	L2,L3
C04	Build UVM testbenches using components like tests, drivers, monitors, and agents.	3	3	3	3	2	-	-	L2,L3
C05	Use UVM sequences and communication ports to send transactions and collect results.	3	3	2	2	2	-	-	L1,L2

Syllabus:

Unit I:

SystemVerilog Fundamentals: Verification Guidelines – Introduction, verification process, basic testbench functionality, testbench components, simulation environment phases, testbench performance. Data Types – built-in data types, arrays, linked lists, creating new types and user defined structures, constants, strings. Procedural Statements and Routines – tasks, functions, and void functions, routine arguments, returning from a routine.Local data storage, time values.

Unit II:

Testbench and OOP Concepts: Connecting the Testbench and Design–separating the testbench and design, the interface construct, stimulus timing, interface driving and sampling, connecting it all together, program-module interactions, SystemVerilog assertions. Basic OOP – define a class, creating new objects, object deallocation, class routines, dynamic objects, copying objects, building a testbench. Randomization – Introduction, randomization in SystemVerilog, constraint details, solution probabilities, valid and in-line constraints, iterative and array constraints, random control, random generators, random device configuration.

Unit-III:

Advanced Concepts for UVM Readiness: Threads and Interprocess Communication – working with threads, interprocess communication, events, semaphores, mailboxes, building testbench with threads and IPC.Advanced OOP and Testbench Guidelines – inheritance, factory patterns, type casting and virtual methods, composition, inheritance, and alternatives, copying an object, callbacks. Functional Coverage – coverage types, strategies, anatomy of a cover group, triggering, data sampling, cross coverage.

Unit-IV:

UVM Infrastructure: Introduction, UVM Components, UVM Tests, UVM Transactions, UVM Sequences

Unit-V:

UVM Integration & TLM (Transaction-Level Modeling) Communication: UVM Agents, Using Analysis Ports in a Testbench, Put and Get Ports in Action, UVM Reporting .

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01, 08th September2025

Approved in ACM No: 01

Text Book

1. Spear, Chris. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. 2nd ed., Springer, 2014.

2. Salemi, Ray. UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology. Mentor Graphics, 2014.

Reference Books

1. Mathur, Ashok B. Advanced Functional Verification: Concepts and Techniques. Springer, 2021.

2. Bhasker, J., and RakeshChadha. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. Prentice Hall, 2007.

3. Bergeron, Janick. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features. 3rd ed., Springer, 2012.

Web References:

1. https://www.doulos.com/knowhow/systemverilog/uvm/uvm-verification-primer/?utm_source=chatgpt.com
2. https://www.chipverify.com/tutorials/uvm?utm_source=chatgpt.com
3. https://colorlesscube.com/uvm-guide-for-beginners/?utm_source=chatgpt.com
4. https://verificationacademy.com/topics/uvm-universal-verification-methodology/?utm_source=chatgpt.com
5. https://www.ibm.com/internet-of-things

eBooks:

1. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features — Spear &Tumbush.
2. The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology — Ray Salemi

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define functional verification in the context of digital design.
- What is the role of SystemVerilog in verification?
- Expand the abbreviation UVM and mention its purpose.
- List any four key features of SystemVerilog used in verification.
- What does constrained random verification (CRV) mean?

L2 – Understand

- Explain the difference between RTL design and functional verification.
- Describe how SystemVerilog classes and OOP concepts support building reusable testbenches.
- Differentiate between code coverage and functional coverage with examples.
- Why are constrained random stimuli important in UVM-based verification?
- Explain the role of UVM factory in creating reusable and configurable verification components.

L3 – Apply

- Write a SystemVerilog class for a simple transaction containing addr, data, and rw fields.
- Develop a constrained random generator in SystemVerilog for generating odd numbers between 1 and 99.
- Apply SystemVerilog assertions (SVA) to check that a signal req is always followed by ack within 2 clock cycles.
- Construct a UVM sequence that sends 10 random read and write transactions to a DUT.
- Demonstrate how to use uvm_config_db to pass configuration objects from a test to an agent.

L4 – Analyze

- Given a UVM testbench with poor coverage results, analyze which components (sequences, monitors, scoreboards, coverage groups) might be missing or incomplete.
- Examine the difference between constrained random verification and directed testing in terms of bug-finding efficiency.
- Debug the following situation: your UVM test finishes prematurely without running all sequences. What possible issues could cause this, and how would you fix them?
- Compare the roles of UVM driver vs. monitor. Why is it important to keep them separate?
- A simulation log shows multiple assertion failures. How would you analyze whether the failures are due to DUT bugs or incorrect assertions?

L5 – Evaluate/Create

- Design a complete UVM testbench architecture for verifying an AXI-based memory controller. Justify your design choices (agents, monitors, scoreboards, sequences, coverage).
- Propose a coverage-driven verification plan for a UART design. Evaluate how you would measure coverage closure and ensure completeness.
- Develop a reusable UVM agent for an SPI protocol and explain how you would integrate it into multiple environments.
- Critically evaluate the use of SystemVerilog Assertions (SVA) vs. functional coverage in ensuring DUT correctness.
- Create a hybrid verification strategy combining directed tests, constrained-random verification, and assertions. Justify how it increases verification efficiency.

Chairperson
Board of Studies (ECE)

R25D57206 LOW POWER VLSI DESIGN3 0 0 3

Course Objectives:

1. Introduce the need for low power design in VLSI systems and its significance in modern electronics.
2. Understand the various sources of power dissipation in digital CMOS circuits.
3. Study different low power design methodologies at circuit, logic, architectural, and system levels.
4. Learn techniques for power estimation, analysis, and optimization in VLSI design.
5. Explore CAD tools and methodologies for low power VLSI design.

Course Outcomes

Course Code	Course Outcomes		MappingwithPOs					
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Identify sources of power dissipation in MOS circuits and explain methods to reduce them.	3	3	2	2	1	-	-	L1,L2
C02	Apply power estimation techniques to valuate energy usage in combinational and sequential logic circuits.	3	3	3	2	1	-	-	L2,L3
C03	Use architectural and circuit-level transformations to optimize designs for low power consumption.	3	3	3	2	2	-	-	L2,L3
C04	Design and test low-voltage CMOS circuits considering submicron effects and leakage currents.	3	3	3	3	2	-	-	L2,L3
C05	Explore and apply advanced low-power techniques such as adiabatic logic and software-level power optimization.	3	3	2	2	2	-	-	L1,L2

Syllabus:

Unit I:

Low-Power CMOS VLSI Design: Introduction, Sources of Power Dissipation, Designing for Low Power. Physics of Power Dissipation in CMOS FET Devices- MIS structure, Long Channel and Sub-micron MOSFET, Gate Induced Drain Leakage, Power dissipation in CMOS-Short Circuit and Dynamic Dissipation, Load Capacitance.

Unit II:

Power Estimation in CMOS Circuits: Modeling of signals, Signal Probability Calculation, Probabilistic Techniques for Signal Activity Estimation. Statistical Techniques - Estimating Average Power in Combinational and Sequential Circuits, Estimation of Glitching Power, Power Estimation using Input Vector Compaction, Power Dissipation in DominoCMOS.

Unit III:

Synthesis for Low Power: Behavioural Level Transforms - Algorithm Level Transforms,Power Constrained Least Squares Optimization for Adaptive and Non-adaptive Filters, Circuit Activity Driven Architectural Transformations, Architecture Driven Voltage Scaling,Power Optimization using Operation Reduction and Substitution, Precomputation-BasedOptimization for Low Power, Logic and Circuit Level Optimization for Low Power.

Unit IV:

Design and Test of Low Voltage CMOS Circuits: Introduction, Circuit Design Styles, Leakage Current in Deep Sub-micrometer Transistors, Deep Sub-micrometer Device DesignIssues, Minimizing Short Channel Effect, Low Voltage Circuit Design Techniques – ReverseVgs, Steeper Sub threshold Swing, Multiple Threshold Voltages, Multiple Supply Voltages.

Unit V:

Advanced Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits. Software Design for Low Power: Introduction, Sources of SoftwarePower Dissipation, Software Power Estimation and Optimization.

Board of Studies: Electronics and Communication Engineering

Approved in BOS No:01, 08th September2025

Approved in ACM No: 01

Text Book

1. Roy, Kaushik, and Sharat C. Prasad. Low-Power CMOS VLSI Circuit Design. Wiley-IEEE Press, 2000.

2. Rabaey, Jan M., Anantha Chandrakasan, and Borivoje Nikolic. Digital Integrated Circuits: A Design Perspective. 2nd ed., Prentice Hall, 2003.

Reference Books

1. Chandrakasan, Anantha P., and Robert W. Brodersen. Low Power Digital CMOS Design. Kluwer Academic Publishers, 1995.

2. Pedram, Massoud. Power-Aware Design Methodologies. Springer, 2005.

Web References:

1. https://www.tutorialspoint.com/vlsi_design/vlsi_design_low_power.htm
2. https://vlsiuniverse.blogspot.com/2013/01/sources-of-power-dissipation-in-cmos.html
3. https://www.geeksforgeeks.org/low-power-vlsi-design-techniques
4. https://nptel.ac.in/courses/106/105/106105161
5. https://www.ibm.com/internet-of-things

eBooks:

1. Low-Power Digital VLSI Design: Circuits and Systems – Abdellatif Bellaouar & Mohamed I. Elmasry.
2. Low-Power CMOS VLSI Circuits & Systems

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define power dissipation in CMOS circuits.
- List the different sources of power consumption in digital VLSI circuits.
- What is static power dissipation?
- What is dynamic power dissipation?
- List any two techniques to reduce leakage current in submicron technologies.

L2 – Understand

- Explain why low power design is critical in modern VLSI circuits.
- Describe the difference between static power and dynamic power dissipation.
- Explain how switching activity affects power consumption in CMOS circuits.
- Summarize the role of power estimation techniques in VLSI design.
- Explain the impact of supply voltage scaling on power and performance.

L3 – Apply

- Apply power estimation techniques to calculate the energy consumption of a given CMOS inverter chain.
- Design a 4-bit adder with clock gating and compare its power usage with a conventional design.
- Use supply voltage scaling to analyze the effect on delay and power in a simple combinational logic circuit.
- Apply MTCMOS techniques to a sequential circuit to reduce leakage power.
- Implement a low-power multiplexer using transistor-level optimizations and measure power reduction.

L4 – Analyze

- Analyze the dynamic vs. static power consumption in a CMOS circuit and identify which dominates at different technology nodes.
- Compare the effectiveness of clock gating and power gating for reducing overall power.
- Analyze the impact of threshold voltage scaling (Vth scaling) on leakage and performance.
- Differentiate between multi-Vdd and dynamic voltage scaling (DVS) approaches for power reduction.
- Analyze the trade-offs between low power design and circuit performance in submicron technologies.

L5 – Evaluate/Create

- Evaluate different low-power design methodologies and recommend the most suitable one for battery-powered IoT devices.
- Critically analyze the trade-offs among power, performance, and area (PPA) in a given VLSI design.
- Evaluate the effectiveness of multi-threshold CMOS (MTCMOS) compared to power gating for leakage reduction.
- Justify the choice of supply voltage scaling for ultra-low-power applications, considering performance constraints.
- Recommend the best low-power optimization technique for mobile processors and justify your reasoning.

Chairperson
Board of Studies (ECE)

R25D57207 MICROCHIP FABRICATION TECHNIQUES 3 0 0 3Course Objectives:

1. Introduce the fundamental concepts of semiconductor materials and their role in microchip fabrication.
2. Understand the principles of cleanroom technology and contamination control in fabrication processes.
3. Study the wafer preparation process, including crystal growth, doping, and substrate formation.
4. Learn various lithography techniques for pattern transfer onto semiconductor wafers.
5. Explore thin-film deposition techniques such as CVD, PVD, and epitaxy for device fabrication.

Course Outcomes

CourseCode	Course Outcomes		MappingwithPOs						
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Describe the semiconductor industry landscape and explain the properties of semiconductor materials and wafer preparation techniques.	3	2	2	1	-	-	-	L1,L2
C02	Outline the wafer fabrication process and apply contamination control and productivity improvement methods.	3	3	2	2	1	-	-	L2,L3
C03	Demonstrate understanding of lithog-raphy and patterning processes used in semiconductor manufacturing.	3	3	3	2	1	-	-	L2,L3
C04	Explain advanced lithography techni-ques, doping processes, and thin-film deposition methods for device fabri-cation.	3	3	3	2	2	-	-	L2,L3
C05	Analyze metallization techniques, device evaluation procedures, package-ing methods, and the business conside-rations of wafer fabrication.3	3	3	2	2		-	-	L1,L2

Syllabus:

Unit-I:

Semiconductor Industry and Materials: The Semiconductor Industry, Properties of Semiconductor Materials and Chemicals, Crystal Growth and Silicon Wafer Preparation.

Unit-II:

Wafer Fabrication and Contamination Control: Overview of Wafer Fabrication, Contamination Control, Productivity and Process Yields, Oxidation .

Unit-III:

Lithography Processes – Patterning Steps: The Ten-Step Patterning Process — Surface Preparation to Exposure, The Ten-Step Patterning Process — Developing to Final Inspection .

Unit-IV:

Advanced Lithography, Doping, and Deposition: Advanced Photolithography Processes, Doping, Layer Deposition

Unit-V:

Metallization, Device Evaluation, Business, and Packaging: Metallization, Process and Device Evaluation, The Business of Wafer Fabrication, Introduction to Devices and Integrated CircuitFormation, Introduction to Integrated Circuits, Packaging.

Board of Studies: Electronics and Communication Engineering
Approved in BOS No:01, 08th September2025
Approved in ACM No: 01

Text Books

1. Van Zant, Peter. Microchip Fabrication: A Practical Guide to Semiconductor Processing. 6th ed., McGraw-Hill, 2014.

Reference Books

1. Ghandhi, Sorab K. VLSI Fabrication Principles: Silicon and Gallium Arsenide. 2nd ed., Wiley,1994.

2. Sze, Simon M., and Kwok K. Ng. Physics of Semiconductor Devices. 3rd ed., WileyInterscience, 2006.

3. Streetman, Ben G., and Sanjay Banerjee. Solid State Electronic Devices. 7th ed., Pearson, 2014.

4. Wolf, Stephen, and Richard N. Tauber. Silicon Processing for the VLSI Era. Vol. 1, Lattice Press, 1986.

Web References:

1. https://semiengineering.com/knowledge_centers
2. https://semiconductor.samsung.com/news-events/tech-blog/a-short-introduction-to-semiconductor-fabrication/?utm_source=chatgpt.com
3. https://en.wikipedia.org/wiki/Semiconductor_device_fabrication?utm_source=chatgpt.com
4. https://en.wikipedia.org/wiki/Photolithography?utm_source=chatgpt.com
5. https://en.wikipedia.org/wiki/Planar_process?utm_source=chatgpt.com

eBooks:

1. Microchip Fabrication: A Practical Guide to Semiconductor Processing — Peter Van Zant.
2. Semiconductor Microchips and Fabrication: A Practical Guide to Theory and Manufacturing — Yaguang Lian.

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define semiconductor fabrication.
- List the main steps involved in the microchip fabrication process.
- State the function of a cleanroom in semiconductor manufacturing.
- Recall the properties of silicon that make it suitable for IC fabrication.
- Define photolithography.

L2 – Understand

- Explain why silicon is the most widely used material for microchip fabrication.
- Describe the role of a cleanroom environment in ensuring wafer quality.
- Explain the difference between wet etching and dry etching with examples.
- Summarize the steps involved in the photolithography process.
- Describe how oxidation is used for device isolation in IC fabrication.

L3 – Apply

- Apply the planar process steps to design a simple MOSFET structure.
- Given a wafer with specific contamination levels, suggest cleanroom protocols to restore acceptable quality.
- Use the lithography process to transfer a 2-$\propto$m line pattern onto a silicon wafer and explain the steps.
- Apply wet oxidation to calculate the oxide thickness for a given temperature and time using Deal Groves model.
- Using ion implantation data, determine the required dose and energy to achieve a specific junction depth.

L4 – Analyze

- Analyze the differences between wet oxidation and dry oxidation in terms of growth rate, quality, and applications.
- Compare diffusion and ion implantation techniques for doping in terms of precision, cost, and depth control.
- Break down the photolithography process into its critical steps and analyze how defects can occur at each stage.
- Analyze the impact of etching methods (wet vs. plasma etching) on device scaling and feature integrity.
- Compare physical vapor deposition (PVD) and chemical vapor deposition (CVD) for thin-film growth in IC fabrication.

L5 – Evaluate/Create

- Evaluate the effectiveness of ion implantation compared to diffusion for advanced technology nodes.
- Critically analyze the limitations of optical lithography and justify the shift toward EUV lithography.
- Evaluate the impact of cleanroom class levels (Class 10 vs. Class 1000) on fabrication yield and reliability.
- Judge the suitability of Aluminum vs. Copper metallization for high-performance VLSI chips.
- Recommend the best etching method (wet, RIE, DRIE) for fabricating deep submicron structures.

Chairperson
Board of Studies (ECE)

R25D57208 POWER MANAGEMENT IC DESIGN 3 0 0 3

Course Objectives:

1. Introduce the fundamental concepts of semiconductor materials and their role in microchip fabrication.
2. Understand the principles of clean room technology and contamination control in fabrication processes.
3. Study the wafer preparation process, including crystal growth, doping, and substrate formation.
4. Learn various lithography techniques for pattern transfer onto semiconductor wafers.
5. Explore thin-film deposition techniques such as CVD, PVD, and epitaxy for device fabrication.

Course Outcomes

Course Code	Course Outcomes	Mapping with POs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
C01	Describe the roles, architectures, and functional requirements of Power Management ICs (PMICs) and their application in modern electronic systems.	3	2	2	1	-	-	-	L1,L2
C02	Design linear voltage regulators, including advanced and digital LDOs, considering efficiency,stability, and transient perfor-mance.	3	3	2	2	1	-	-	L2,L3
C03	Analyse inductive DC-DC converter topologies (buck, boost, buck-boost, multi-phase, SIMO) with emphasis on perfor-mance metrics and control techniques.	3	3	3	2	1	-	-	L2,L3
C04	Implement switched capacitor and charge pump converters for integrated, compact, and efficient power management solutions.	3	3	2	2	1	-	-	L2,L3
C05	Integrate gate driver circuits, protection mechanisms, and sensing modules to ensure reliability and safety in PMICs.	3	2	2	1	-	-	-	L1,L2

Syllabus:

Unit-I:

Fundamentals of Power Management ICs: Role and requirements of Power Management ICs (PMICs), the smartphone as a typical example, fundamental concepts - linear regulator, the inductive DC-DC converter, the Switched capacitor converters, the hybrid converter, power delivery - lateral and vertical, integrated voltage regulator (IVR), dynamic voltage and frequency scaling (DVFS).

Unit-II:

Linear Voltage Regulators: Fundamental circuit and control concept, drop voltage and power efficiency, frequency behavior and stability, fast transient techniques and slew-rate enhancement, PSRR, output noise, soft-start, Advanced LDO types: capacitor-less, flipped voltage follower,

Digital LDOs: ADC, digital controller, limit cycle oscillations.

Unit-III:

Inductive DC-DC Converters: The fundamental Buck converter, voltage conversion ratio, ripple, losses and power conversion efficiency, inductor and capacitor sizing, voltage-mode and current mode control, Loop compensation: Type I, II, III compensators, Constant on-time and hysteretic control, DCM operation and burst mode, Boost, buck-boost, and flyback converters, Multi-phase converters: ripple cancellation, phase shedding, Single inductor multiple output (SIMO) converters.

Unit-IV:

Switched-Capacitor (SC) and Charge Pump Converters: Basic operation of charge pumps: diode-based and transistor-based, Parasitic effects, charge sharing, and efficiency, SC converter topologies: Dickson, ladder, Fibonacci, Charge flow modeling and output resistance, Gate drive techniques, Capacitor and switch sizing, multi-phase and multi-ratio SC converters, interleaving, ripple reduction, and closed-loop control.

Unit-V:

Gate Drivers, Protection, and Sensing: Gate driver architectures: CMOS inverters, cascaded drivers, Bootstrap techniques and dv/dt triggering, Level shifters: resistor-based, cross-coupled, capacitive, Current sensing methods: shunt, replica, DCR, Protection circuits: OVP, thermal shutdown, UVLO, power-on-reset, Bandgap reference circuits and trimming, Zero-cross detection and current limiting.

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Approved in BOS No: 01, 08th September2025

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Text Books

1. Wicht, Bernhard. Design of Power Management Integrated Circuits. Wiley, 2024.

Reference Books

1. Erickson, Robert W., and Dragan Maksimovic. Fundamentals of Power Electronics. 2nd ed. Springer, 2001.

2. Basso, Christophe. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs. McGraw-Hill Education, 2008.

3. Wu, Jinrong, and Ray Ridley. Power Supply Design: A Practical Guide. Springer, 2019.

Web References:

1. https://reversepcb.com/pmic/?utm_source=chatgpt.com
2. https://www.cytechsystems.com/news/pmics-guide?utm_source=chatgpt.com
3. https://resources.pcb.cadence.com/blog/2023-challenges-in-power-management-ic-pmic-design?utm_source=chatgpt.com
4. https://www.eeworldonline.com/power-management-ics-part-1-pmic-functions/?utm_source=chatgpt.com
5. https://jlcpcb.com/blog/what-is-a-power-management-ic?utm_source=chatgpt.com

eBooks:

1. Design of Power Management Integrated Circuits — Bernhard Wicht
2. Power Management Integrated Circuits — Mona M. Hella& Patrick Mercier

Internal Assessment Pattern

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	20%	15%
L2	30%	25%
L3	35%	40%
L4	10%	15%
L5	5%	5%
Total (%)	**100**	**100**

Sample Questions by Cognitive Level

L1 – Remember

- Define a Power Management Integrated Circuit (PMIC).
- List the main functions of PMICs in modern electronic systems.
- State the difference between a linear regulator and a switching regulator.
- Identify the basic blocks of a Low Dropout Regulator (LDO).
- Recall the meaning of PPA trade-offs in PMIC design.

L2 – Understand

- Explain the importance of PMICs in portable electronic devices like smartphones and IoT systems.
- Differentiate between analog LDOs and digital LDOs in terms of architecture and performance.
- Summarize the role of DC-DC converters in improving efficiency compared to linear regulators.
- Explain why multi-phase buck converters are used in high-current applications such as CPUs and GPUs.
- Illustrate with a block diagram the operation of a switched-capacitor (charge pump) converter.

L3 – Apply

- Design a basic LDO regulator circuit to provide 1.2 V output from a 3.3 V supply.
- Apply Ohm□s law and power equations to calculate the efficiency of a linear regulator supplying 1 A at 1.8 V from a 5 V input.
- Demonstrate how to size an inductor for a buck converter supplying 2 A load current.
- Implement a simple charge pump circuit to double the input voltage (e.g., 3.3 V □ 6.6 V).
- Use a multi-phase buck converter design to show how current sharing improves thermal performance.

L4 – Analyze

- Analyze the trade-offs between linear regulators and switching regulators in terms of efficiency, noise, and area.
- Examine the impact of output capacitor ESR on the stability of an LDO regulator.
- Compare the performance of a buck converter vs. a SIMO converter in powering multiple SoC rails.
- Break down the sources of power loss in inductive DC-DC converters (switching loss, conduction loss, core loss).
- Analyze why multi-phase buck converters provide better thermal and current-handling performance than single-phase designs.

L5 – Evaluate/Create

- Evaluate the suitability of a multi-phase buck converter for powering modern CPUs versus GPUs.
- Critically analyze the limitations of switched-capacitor converters compared to inductive converters for high-current applications.
- Judge the effectiveness of digital LDOs in ultra-low-power IoT devices compared to analog LDOs.
- Recommend the best converter topology (buck, boost, buck-boost, SIMO) for a wearable medical device and justify your choice.
- Evaluate the trade-offs between efficiency and noise performance in choosing linear regulators for RF circuits.

Chairperson
Board of Studies (ECE)

R25D57209 MIXED SIGNAL IC DESIGN LAB 0 04 2

Course Objectives

1.Introduce Signal Representation Techniques
2.Develop Understanding of Digital Signal Processing Blocks
3.Expose to Sampling and Data Conversion Principles**.**
4.Integrate Analog and Mixed-Signal Circuit Design Concepts
5.Analyze Frequency and Time Domain Behavior of Systems

Course Code	Course Outcomes	MappingwithPOs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
CO1	Analyze and represent signals using sinusoidal components and the complex z-plane.	3	2	1	1	1	-	-	L1, L3
CO2	Design and evaluate sample-and-hold circuits and interpolation techniques to mitigate aliasing effects.	3	2	3	2	1	1	-	L3, L4
CO3	Implement and analyze analog filter circuits including active-RC, MOSFET-C, and gm-C integrators.	3	3	2	2	2	-	2	L3, L4
CO4	Design and simulate digital filters such as comb, Sinc-shaped, and FIR filters using bilinear transform methods.	1	3	2	-	-	2	3	L3, L4
CO5	Model and evaluate the performance of data converters including ideal DACs and ADCs.	2	1	2	-	3	-	1	L2,L5

ListofExperiments:

1.**Sinusoidal Signals and Quadrature Components**: Generate and analyze sinusoidal signals including their in-phase and quadrature components to understand signal representation.

2. **Signal Representation on Complex (z-) Plane**: Plot signals on the complex z-plane and analyze their magnitude and phase characteristics.

3. **Digital Comb Filter Design**: Design and simulate a digital comb filter and analyze its frequency response to understand notch filtering.

4. **Digital Differentiator and Integrator**: Implement digital differentiator and integrator circuits and analyze their time and frequency domain responses.

5. **Impulse Sampling and Aliasing Analysis**: Simulate impulse sampling and study the aliasing effect in the frequency spectrum of the sampled signal.

6. **Sample-and-Hold (S/H) Circuit Analysis**: Design a sample-and-hold circuit and analyze its spectral response and effect on signal reconstruction.

7. **Interpolation Techniques**: Implement zero padding and linear interpolation methods on sampled data to improve signal resolution.
8. **Switched-Capacitor Sample-and-Hold Circuit**: Design a switched-capacitor sample-and hold circuit with non-overlapping clocks and analyze its performance.
9. **Active-RC Low-Pass Integrator Design**: Design and simulate an active-RC low-pass integrator filter and analyze its frequency response.
10. **MOSFET-C and gm-C Integrator Design**: Implement MOSFET-C and gm-C integrators, compare their characteristics and frequency response.
11. **Discrete-Time Integrator Design**: Design and analyze discrete-time integrator circuits to understand their filtering behavior.
12. **Ideal DAC and ADC Modeling**: Model ideal DAC and ADC circuits, and analyze their input output characteristics and linearity.
13. **Sinc-Shaped Digital Filter Design**: Design Sinc-shaped digital filters including bandpass and highpass filters and analyze their frequency response.
14. **FIR Filter Implementation Using Bilinear Transfer Function**: Implement FIR filters using the bilinear transfer function and analyze filter characteristics like gain and phase response.

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Approved in ACM No: 01

Web References

- NPTEL – https://nptel.ac.in/courses/dsd design/108/105/108105158/
- Tutorials: https://www.electronics-tutorials.ws/
- All About Circuits: https://www.allaboutcircuits.com/
- https://www.CMRR similation 4u.com/
- Virtual Labs – https://vlab.amrita with plds.edu/

E-Books

- CMOS Mixed-Signal Circuit Design (Second Edition)
- The Scientist and Engineer's Guide to Digital Signal Processing (Steven W. Smith)
- Analog & Mixed-Signal Electronics by Karl D. Stephan

Internal Assessment Pattern Sample

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	10%	5%
L2	20%	15%
L3	40%	40%
L4	30%	40%
L5	—	—
Total (%)	**100**	**100**

Questions by Cognitive Level

L1 – Recall (Short Answer)

1. Define in-phase and quadrature components of a sinusoidal signal.
2. What is aliasing in sampled signals?
3. List the types of digital filters studied in the lab.
4. State the function of a sample-and-hold circuit.
5. Define Sinc filter and its application

L2 – Understand (SA/LA)

1. Explain how signals are represented on the complex z-plane.
2. Describe the working principle of a digital comb filter.
3. Differentiate between a digital differentiator and digital integrator.
4. Summarize the effect of interpolation on resolution.
5. Explain the difference between MOSFET-C and gm-C integrators.

L3 – Apply (LA)

1. Generate and plot quadrature components of a sinusoidal signal using MATLAB/Simulink.
2. Apply impulse sampling to a signal and study the aliasing effect in the frequency domain.
3. Implement a zero-padding method for interpolation and compare the results with linear interpolation.
4. Design and simulate an active-RC integrator and measure its frequency response.
5. Model an ideal ADC and verify its input-output linearity.

L4 – Analyze (LA)

1. Analyze the magnitude and phase characteristics of a signal on the z-plane.
2. Compare the frequency responses of digital comb filters and Sinc-shaped filters.
3. Examine the performance of switched-capacitor vs conventional sample-and-hold circuits.
4. Analyze the time-domain response of discrete-time integrators.
5. Investigate the distortion effects caused by aliasing in impulse-sampled signals.

L4 – Analyze (LA)

1. Evaluate the trade-offs between active-RC and MOSFET-C integrator designs.
2. Assess the performance of FIR filters implemented using bilinear transfer function.
3. Judge which interpolation method (zero padding vs linear) is more effective for signal reconstruction.
4. Validate the spectral response of a sample-and-hold circuit against theoretical expectations.
5. Critique the linearity performance of ideal ADC and DAC models.

Chairperson
Board of Studies (ECE)

R25D57210 FPGA BASED SYSTEM DESIGN LAB 0 0 4 2

Course Objectives

1.Provide hands-on experience in developing testbenches with constrained random verification, coverage, and assertions.
2.Familiarize students with object-oriented programming concepts in SystemVerilog for building reusable verification components.
3.Enable students to perform coverage-driven verification for complex digital designs.
4.Train students in using industry-standard simulators and EDA tools to implement UVM-based verification environments.
5.Encourage team-based project work to verify RTL designs using advanced verification methodologies.

Course Code	Course Outcomes	MappingwithPOs							
		PO1	PO2	PO3	P04	P05	P06	P011	Dok
CO1	Write and simulate HDL code for basic combinational and sequential digital circuits using Verilog HDL.	3	2	1	1	1	-	-	L1, L3
CO2	Design and implement complex digital systems such as FSMs, arithmetic logic units, and communication modules on FPGA platforms.	3	2	3	3	1	1	-	L3, L4
CO3	Develop and verify interfacing protocols for external hardware devices like seven-segment displays, keypads, and UART communication	3	3	1	2	2	-	2	L2, L4
CO4	Apply design methodologies for timing, synchronization, and resource optimization in FPGA based digital system design.	1	3	1	-	-	2	3	L1, L4
CO5	Demonstrate the ability to deploy and debug digital designs on FPGA development boards, validating functionality through hardware testing.	3	1	1	-	3	-	1	L2,L5

ListofExperiments:(Any 12 Experiments)

1. **LED Blinking Using Verilog**: Implement a basic LED blink circuit to understand FPGA programming and output pin control.
2. **Design and Simulation of Basic Logic Gates using Verilog HDL**: To write HDL code for basic logic gates (AND, OR, NOT, XOR), simulate their functionality, and verify the outputs using a waveform viewer.
3. **Implementation of 4-bit Adder/Subtractor on FPGA**: To design and implement a 4-bit adder/subtractor using Verilog, simulate and verify functionality on an FPGA development board.
4. **Design of a 4x1 Multiplexer and 1x4 Demultiplexer**: To write and simulate Verilog code for a 4x1 MUX and 1x4 DEMUX and validate outputs through FPGA implementation.

5. **Comparator Design (2-bit or 4-bit):** Design a simple digital comparator circuit that compares two binary inputs.

6. **Design and Implementation of a 4-bit Synchronous Counter**: To implement a 4-bit up/down synchronous counter using HDL, simulate for timing and logic correctness, and deploy it on FPGA hardware.

7. **Finite State Machine (FSM) Design**: Sequence Detector-To design a Moore or Mealy FSM for sequence detection, simulate the state transitions, and implement the design on an FPGA board.

8. **Design and Implementation of an ALU Supporting Basic Operations**: To design an Arithmetic Logic Unit that performs basic arithmetic and logic functions (ADD, SUB, AND, OR, NOT) and test it on FPGA.

9. **Interfacing Seven Segment Display with FPGA**: To write HDL code to drive a seven segment display with binary or BCD inputs and implement the interface on FPGA hardware.10. **Shift Register (Left/Right**): Design a shift register that shifts input bits left or right on each clock pulse.

11. **Implementation of Traffic Light Controller using FSM on FPGA**: To design a traffic light controller using finite state machines, simulate its time sequence, and implement it on FPGA hardware.

12. **PWM Signal Generation using FPGA**: To implement a pulse-width modulation (PWM) generator using Verilog HDL and demonstrate its use in applications like LED brightness control.

13. **Real-Time Clock Design and Display using FPGA**: To implement a real-time clock on FPGA with hour-minute-second display and use multiplexed seven-segment display for output.

14. **Serial Input with UART Receiver (Basic):**Implement a simple UART receiver to receive serial data and blink an LED.

15. **Implementing Digital Filters (FIR/IIR) on FPGA**: To implement a basic Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter in HDL and simulate its output for given inputs.

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Web References

- NPTEL – https://nptel.ac.in/courses/FPGA design/108/105/108105158/
- Tutorials: https://www.electronics-tutorials.ws/
- All About Circuits: https://www.allaboutcircuits.com/
- https://www.RTOSsimulation 4u.com/
- Virtual Labs – https://vlab.amrita with FPGA.edu/

E-Books

- Digital Systems Design Using Verilog (Roth, John & Lee)
- Fundamentals of Digital Logic with Verilog Design (3rd Edition)
- Design Recipes for FPGAs Using Verilog and VHDL (Peter Wilson)

Internal Assessment Pattern Sample

Cognitive Level	Internal Assessment #1(%)	Internal Assessment #2(%)
L1	10%	5%
L2	20%	15%

L3	40%	40%
L4	30%	40%
L5	—	—
Total (%)	**100**	**100**

Questions by Cognitive Level

L1 – Recall (Short Answer)

1. Define Verilog HDL.
2. List the different data types available in Verilog.
3. What is the function of a reg and a wire in Verilog?
4. Recall the difference between blocking (=) and non-blocking (<=) assignments.
5. State the applications of FPGA in digital system design.

L2 – Understand (SA/LA)

1. Explain the working principle of an FPGA-based LED blinking circuit.
2. Differentiate between synchronous and asynchronous counters.
3. Interpret the difference between Moore and Mealy FSMs with an example.
4. Explain how a 7-segment display is interfaced with FPGA using Verilog.
5. Describe how PWM can be used to control LED brightness.

L3 – Apply (LA)

1. Write Verilog code for a 4x1 multiplexer and test it using a waveform simulation.
2. Implement a 4-bit comparator in Verilog and demonstrate its functionality.
3. Apply FSM design concepts to implement a sequence detector for "1011".
4. Develop Verilog code for a 4-bit synchronous up/down counter.
5. Use an FPGA board to interface UART and verify received serial data.

L4 – Analyze (LA)

1. Compare the design flow of a 4-bit adder using structural modeling vs behavioral modeling in Verilog.
2. Analyze the timing diagram of a synchronous counter implemented on FPGA.
3. Differentiate between FSM-based traffic light controller and hardwired controller.
4. Identify the impact of propagation delay in a 7-segment display driver circuit.
5. Analyze the resource utilization (LUTs, flip-flops) of an ALU design on FPGA.

L5 – Analyze (LA)

1. Justify the need for using FPGAs instead of microcontrollers for real-time clock design.
2. Evaluate the performance differences between FIR and IIR filter implementations on FPGA.
3. Critically examine the effectiveness of Verilog testbenches in debugging hardware designs.
4. Assess the reliability of UART communication in FPGA systems under noisy conditions.
5. Compare various FPGA families (Xilinx, Intel/Altera) for suitability in digital system prototyping.

Chairperson
Board of Studies (ECE)

R25MBA201 **Constitution of India** **2 0 0 0**

(M. Tech Computer Science and Engineering)

Course Objectives: Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

SYLLABUS

UNIT-I:

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working), Philosophy of the Indian Constitution: Preamble, Salient Features.

UNIT-II:

Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT-III:

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.

2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.

3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.

4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Chairperson
Board of Studies (MBA)

R25MBA202 **Pedagogy Studies** **2 0 0 0**

(M. Tech Computer Science and Engineering)

Course Objectives: Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

SYLLABUS

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

UNIT-V:

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.

2. Agrawal M (2004) curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.

3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.

5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.

6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.

7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Chairperson
Board of Studies (MBA)